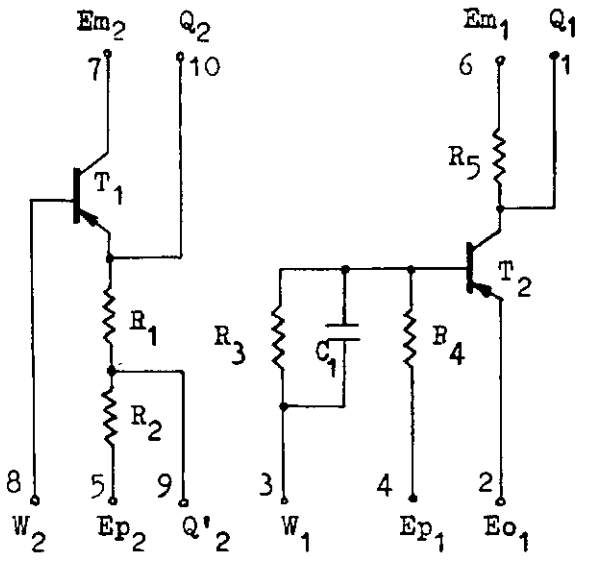
# MULLARD COMBI ELEMENTS

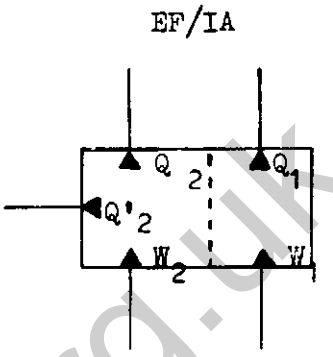
These pages have data from 1963 on the various blocks marketed by Mullard Equipment Ltd.

A separate pdf file is available with general data and developer and mounting hardware.

# EMITTER FOLLOWER/INVERTER AMPLIFIER

EF/IA1 B8 940 00
B1 649 07




TERMINAL INDICATION

Pin

| | | | | |
|---|---|---|---|---|
| 1 | = | $Q_1$ | = | Output 1 |
| 2 | = | $Eo_1$ | = | Common supply terminal (O V) |
| 3 | = | $W_1$ | = | Input 1 |
| 4 | = | $Ep_1$ | = | Positive supply terminal (+ 6 V) |
| 5 | = | $Ep_2$ | = | " " " " |
| 6 | = | $Em_1$ | = | Negative " " (- 6 V) |
| 7 | = | $Em_2$ | = | " " " " |
| 8 | = | $W_2$ | = | Input 2 |
| 9 | = | $Q'_2$ | = | Tapped output 2 |
| 10 | = | $Q_2$ | = | Direct output 2 |

Note : The terminals indicated by a 1 belong to the inverter amplifier; the terminals indicated by a 2 belong to the emitter follower.

This unit comprises the standard EF and IA circuits, which can be used independently. For further data see the Twin Emitter Follower and Twin Inverter Amplifier sheets.

When both circuits in this unit are suitably interconnected, an inverting amplifier can be obtained which provides fast level transitions in both directions, at a heavy capacitive load.

POWER REQUIREMENTS

| | | | |
|---|---|---|---|
| Pin 2 | Eo | = | 0 V |
| Pins 6,7 | Em | = | - 6 V ± 10 % (3.3 - 12.6) mA |
| Pins 4,5 | Ep | = | + 6 V ± 10 % (3.5 - 6.8) mA |

Deviations given are permitted in all combinations.

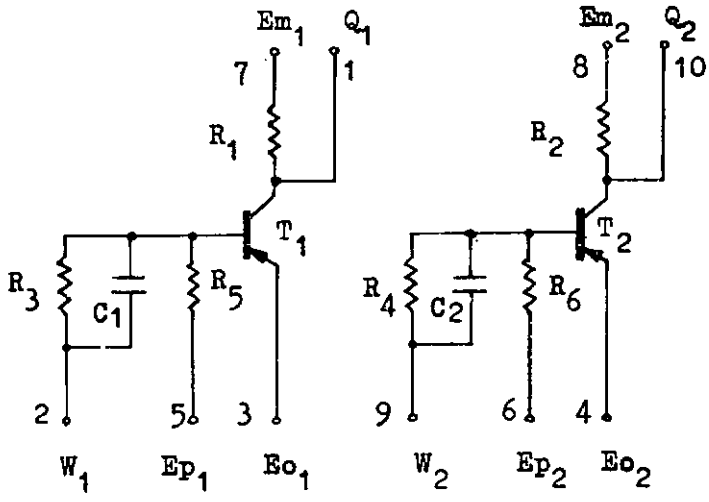


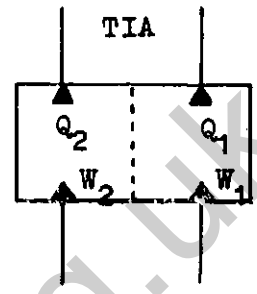


MULLARD EQUIPMENT LIMITED
A COMPANY OF THE MULLARD GROUP

# TWIN INVERTER AMPLIFIER 21A1

B8 940 02
B1 649 10




TERMINAL INDICATION

Pin

| | | | | |
|---|---|---|---|---|
| 1 | = | $Q_1$ | = | Output 1 |
| 2 | = | $W_1$ | = | Input 1 |
| 3 | = | $Eo_1$ | = | Common supply terminal (0 V) |
| 4 | = | $Eo_2$ | = | " " " " |
| 5 | = | $Ep_1$ | = | Positive " " (+ 6 V) |
| 6 | = | $Ep_2$ | = | " " " " |
| 7 | = | $Em_1$ | = | Negative " " (- 6 V) |
| 8 | = | $Em_2$ | = | " " " " |
| 9 | = | $W_2$ | = | Input 2 |
| 10 | = | $Q_2$ | = | Output 2 |

POWER REQUIREMENTS

Pins 3,4 Eo = 0 V
Pins 7,8 Em = - 6 V ± 10 % 2 x (0 - 6) mA
Pins 5,6 Ep = + 6 V ± 10 % 2 x 0.12 mA
Deviations given are permitted in all combinations.

OUTPUT CHARACTERISTICS

($Q_1$ and $Q_2$ terminals)

a) Output levels (at full load)
binary "0" < |-0.2| V
binary "1" > | 0.7 Em| V.

b) Permissible maximum load currents :
at "0" level - 2.5 mA
at "1" level + 1.6 mA

c) Typical maximum capacitive load at high speed operation :
2000 pF



MULLARD EQUIPMENT LIMITED
A COMPANY OF THE MULLARD GROUP

d) Output impedance (approximate values)

| | D.C. (resistive) load : | A.C. (capacitive) load : |
|---|---|---|
| at "0" level : | 50 Ω | 100 Ω for positive going step |
| at "1" level : | 1000 Ω | 1000 Ω for negative going step |

INPUT CHARACTERISTICS

D.C. input : negative going voltage level applied to $W_1$ or $W_2$.

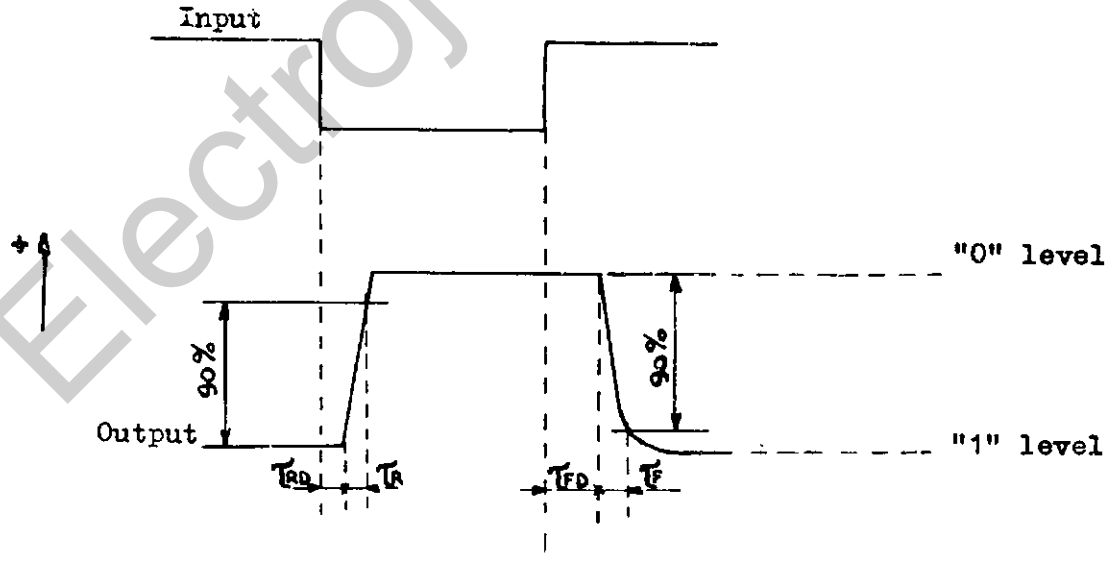
| | |
|---|---|
| Necessary maximum amplitude : | 0.6 Em V. |
| Permissible maximum amplitude : | - 10 V. |
| Input impedance static : | > 7000 Ω. |
| Input impedance dynamic : equivalent to a capacity of about | 400 pF |
| Permissible maximum positive voltage : | 10 V. |
| Permissible maximum input noise : | - 0.3 V. |

SWITCHING TIMES

Input signal : negative going voltage step.
At the outputs $Q_1$ and $Q_2$, unloaded :

| | |
|---|---|
| Rise time, $\tau_R$ | < 0.3 µsec |
| Rise delay time, $\tau_{RD}$ | < 0.1 µsec |
| Fall time, $\tau_F$ | < 2 µsec |
| Fall delay time, $\tau_{FD}$ | < 0.6 µsec |

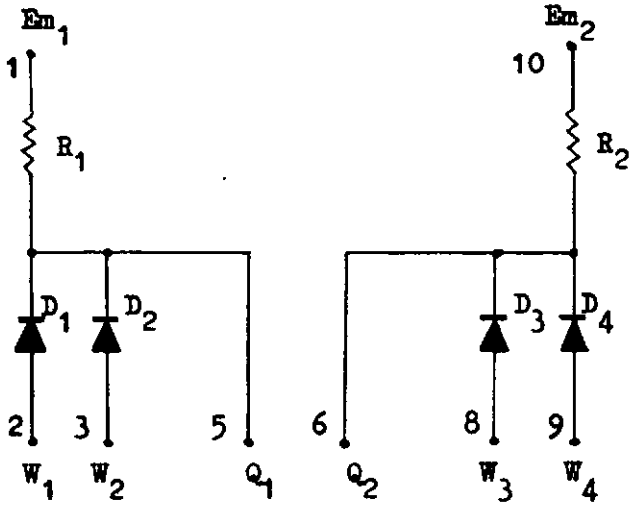
Explanation of these notations :

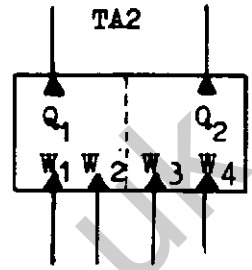



FREQUENCY RANGE 0 - 100 kc/s

# TWIN 2-INPUT AND GATE 22A1

B8 930 01
B1 649 04




TERMINAL INDICATION

| Pin | | | |
|---|---|---|---|
| 1 | = $Em_1$ | = | Negative supply terminal (- 6 V) |
| 2 | = $W_1$ | = | Input 1 |
| 3 | = $W_2$ | = | " 2 |
| 4 | = | = | n.c. (not connected) |
| 5 | = $Q_1$ | = | Output 1 |
| 6 | = $Q_2$ | = | " 2 |
| 7 | = | = | n.c. |
| 8 | = $W_3$ | = | Input 3 |
| 9 | = $W_4$ | = | " 4 |
| 10 | = $Em_2$ | = | Negative supply terminal (- 6 V) |

POWER REQUIREMENTS

Pins 1,10 Em = - 6 V ± 10 % 2 x (0 - 0.5) mA

Deviations given are permitted in all combinations.

OUTPUT CHARACTERISTICS

($Q_1$ and $Q_2$ terminals)

a) Output levels (unloaded)
binary "0" : maximum 0.35 V more negative than the input voltage level.
binary "1" : equal to the lowest input voltage level.

b) Available output current
at "0" level : not customary to use any
at "1" level : 0.35 mA

c) Output impedance : < 13 kΩ

## INPUT CHARACTERISTICS

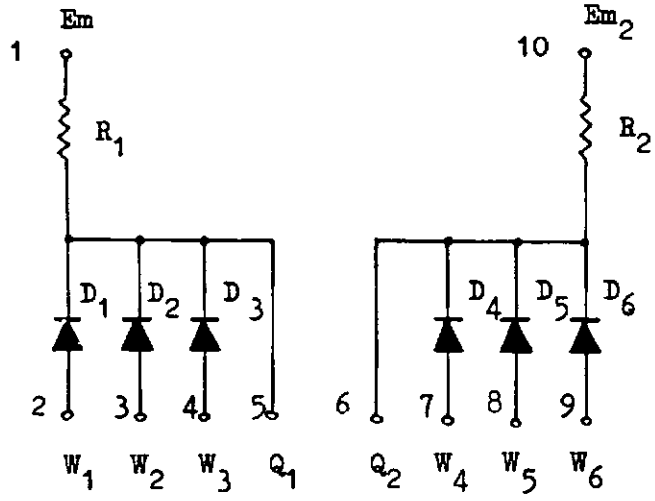
D.C. inputs applied to $W_1$, $W_2$ and $W_3$, $W_4$.

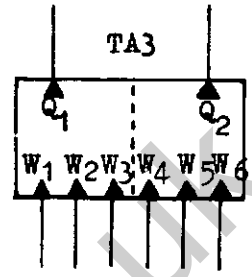
Maximum input current :

at "0" level : + 0.6 mA
at "1" level : - 0.03 mA

# TWIN 3-INPUT AND GATE 23A1

B8 930 00
B1 649 03




## TERMINAL INDICATION

| Pin | | | | |
|---|---|---|---|---|
| 1 | = | Em | = | Negative supply terminal (- 6 V) |
| 2 | = | $W_1$ | = | Input 1 |
| 3 | = | $W_2$ | = | " 2 |
| 4 | = | $W_3$ | = | " 3 |
| 5 | = | $Q_1$ | = | Output 1 |
| 6 | = | $Q_2$ | = | " 2 |
| 7 | = | $W_4$ | = | Input 4 |
| 8 | = | $W_5$ | = | " 5 |
| 9 | = | $W_6$ | = | " 6 |
| 10 | = | $W_7$ | = | Negative supply terminal (- 6 V) |

## POWER REQUIREMENTS

Pins 1,10 Em = - 6 V ± 10 % 2 x (0 - 0.5) mA

Deviations given are permitted in all combinations.

## OUTPUT CHARACTERISTICS

($Q_1$ and $Q_2$ terminals)

a) Output levels (unloaded)
binary "0" : maximum 0.35 V more negative than the input voltage level.
binary "1" : equal to the lowest input voltage level.

b) Available output current:
at "0" level : not customary to use any
at "1" level : 0.35 mA

c) Input impedance : ◅ 13 kΩ





MULLARD EQUIPMENT LIMITED
A COMPANY OF THE MULLARD GROUP

## INPUT CHARACTERISTICS

D.C. inputs applied to $W_1$ - $W_3$ and $W_4$ - $W_6$

Maximum input current:

| | |
|---|---|
| at "0" level | + 0.6 mA |
| at "1" level | - 0.03 mA |

# TWIN INVERTER AMPLIFIER 2IA2

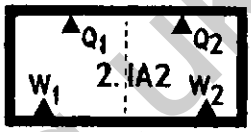
B8 940 05

COLOUR CODE YELLOW

## DATA SHEET

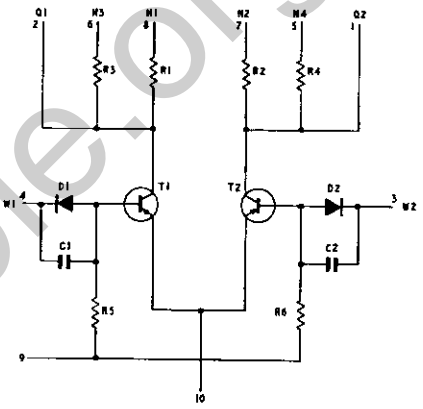
Unit B8 940 05 contains two identical IA2 transistor-inverter amplifier circuits. The circuits combine an inverting function with an appreciable power amplification between input and output. The unit has been designed specially to amplify the weak output signals originating from a diode-gate circuit, but it can also be used as a drive for power stages.

Frequency range: 0–100 kc/s
Ambient temperature: –20 to + 60° C
Weight: 21 g approximately




Circuit Data

Terminal 1 = $Q_2$ = output 2
2 = $Q_1$ = output 1
3 = $W_2$ = input 2
4 = $W_1$ = input 1
5 = $N_4$ = supply – 6V[1]
6 = $N_3$ = supply – 6V[1]
7 = $N_2$ = supply – 6V[1]
8 = $N_1$ = supply – 6V[1]
9 = +6V
10 = E = common supply 0V




POWER SUPPLY

Terminal 5: $N_4$ = –6V ± 10%, $-I_{N4}$ = 0–4 mA
6: $N_3$ = –6V ± 10%, $-I_{N3}$ = 0–4 mA
7: $N_2$ = –6V ± 10%, $-I_{N2}$ = 0–2 mA
8: $N_1$ = –6V ± 10%, $-I_{N1}$ = 0–2 mA
9: P = +6V ± 10% $I_p$ = 0–2 mA
10: E = 0 V common

Nominal value of the current

INPUT SIGNAL DATA (W input) [2]

APPLICATION 1. (Used as a gate amplifier): IA2 after a standard AND gate or a standard AND gate followed by a standard OR gate circuit. In the latter case the P Supply of the gate may be left floating.

Transistor Conducting

Input current: $-I_W$ = 0.3mA minimum

(Under these drive conditions the input voltage will reach a value -1V

Transistor Non-conducting

Input voltage: 0.2V minimum

APPLICATION 2, (Used as a power amplifier): IA2 driven by a grounded-emitter stage with a collector resistance of 1kΩ, connected to the -6V supply terminal. This driving stage can be a standard IA1 circuit (incorporated in the units B8 940 00 and B8 940 02) or another IA2 circuit with both corresponding -6V supply terminals connected to the negative supply line. In both cases the collector (Q) terminal of the driving stage is connected directly to the W terminal of the IA2.

Transistor Conducting

Input current $-I_W$ = 3.7mA minimum

(Under these drive conditions the input voltage will reach a value $-V_{WD}$ = 1.3V maximum.)

LIMITING VALUES:

$-I_W$ = 10 mA maximum

$V_W$ = 10 V maximum

OUTPUT DATA [2]

APPLICATION 1. (see previous description)

Transistor conducting:

Output current = $I_Q$ = 5.5 mA maximum [3]

$I_Q$ = 3.6 mA maximum [4]

$I_Q$ = 0 mA maximum [5]

Output voltage $V_Q$ = 0.2 V maximum

Transistor Non-conducting:

Output current = $I_Q$ = 0 mA maximum [3]

$I_Q$ = 0.49 mA maximum [4]

$I_Q$ = 1.5 mA maximum [5]

Output voltage $-V_Q$ = 3.8 V minimum

APPLICATION 2. (see previous description)

Transistor Conducting:

Output current $-I_Q$ = 80 mA maximum [3]
= 74 mA maximum [5]

Output voltage $-V_Q$ = 0.25V maximum

Transistor Non-conducting:

Output current $I_Q$ = 0 mA maximum
$I_Q$ = 1.5 mA maximum [5]

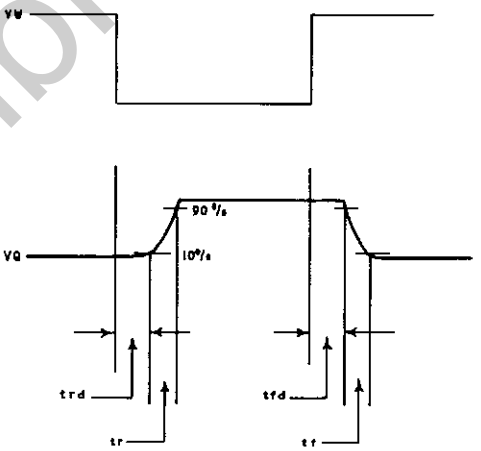
Output voltage $-V_Q$ = 3.8V minimum

Switching and Delay Times

As a gate amplifier (refer to application 1) the unit is driven from a square-wave voltage source via a standard AND gate, followed by a standard OR gate.

UNIT UNLOADED

| | | |
|---|---|---|
| Rise delay | $t_{rd}$ | = 0.2 $\mu$ s maximum |
| Rise time | $t_r$ | = 1.5 $\mu$ s maximum |
| Fall delay | $t_{fd}$ | = 1 $\mu$ s maximum |
| Fall time | $t_f$ | = 2.5 $\mu$ s maximum |




OUTPUT IMPEDANCE

Positive-going output voltage $R_i$ = 100 $\Omega$
Negative-going output voltage $R_i$ = 1000 $\Omega$ [5]

Notes:

Use dependent on application.

This data applies only to the most adverse working conditions for a combination of units – namely to supply voltages $V_N$ = -5.4 V and $V_p$ = +6.6 V. Unless specified to the contrary, all voltage and current figures quoted represent absolute maximum values.

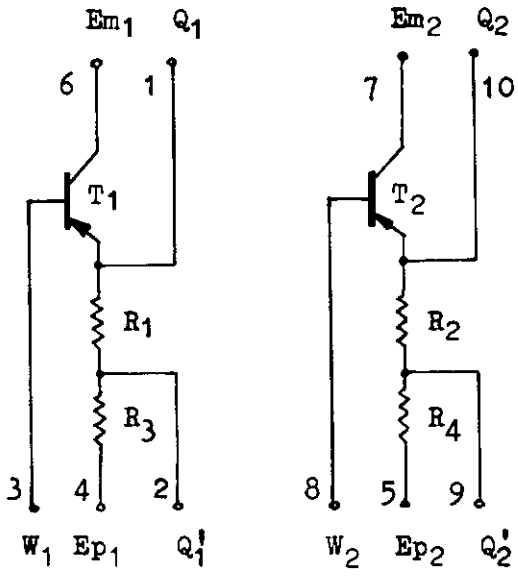
With all N terminals floating.

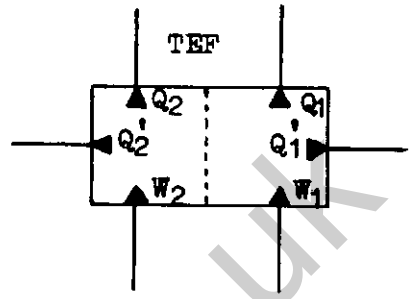
With terminals N1 or N2 connected to the -6V supply.

With terminals N1 and N3 or N2 and N4 connected to the -6V supply.

# TWIN EMITTER FOLLOWER 2EF1

B8 940 01
B1 649 09




TERMINAL INDICATION

Pin

| | | | | |
|---|---|---|---|---|
| 1 | = | $Q_1$ | = | Direct output 1 |
| 2 | = | $Q_1'$ | = | Tapped output 1 |
| 3 | = | $W_1$ | = | Input 1 |
| 4 | = | $Ep_1$ | = | Positive supply terminal (+ 6 V.) |
| 5 | = | $Ep_2$ | = | " " " " |
| 6 | = | $Em_1$ | = | Negative " " (- 6 V.) |
| 7 | = | $Em_2$ | = | " " " " |
| 8 | = | $W_2$ | = | Input 2 |
| 9 | = | $Q_2'$ | = | Tapped output 2 |
| 10 | = | $Q_2$ | = | Direct output 2 |

The $Q_1'$ and $Q_2'$ terminals provide a positive bias voltage in the binary "0" state.

POWER REQUIREMENTS

Pins 6,7 Em = - 6 V ± 10 % 2 x (3.3 - 6.6) mA.
Pins 4,5 Ep = + 6 V ± 10 % 2 x (3.3 - 6.6) mA.

Deviations given are permitted in all combinations.

OUTPUT CHARACTERISTICS

($Q_1$ and $Q_2$ terminals)

a) Output levels (at full load).
binary "0" : maximum 0.4 V more positive than the input level.
binary "1" : > |0.7 Em| V, when loaded in accordance with the details in the next paragraph.

b) Permissible maximum load currents : (under conditions given in the next paragraph)
at "0" level : - 2.5 mA
at "1" level : + 4 mA



MULLARD EQUIPMENT LIMITED
A COMPANY OF THE MULLARD GROUP

Maximum load currents on $Q_1$ and $Q_2$ when driven by a :

| | |
|---|---|
| flip-flop | 4 mA |
| one-shot | 4 mA |
| pulse shaper | 6 mA |
| inverter | 10 mA |

c) Typical maximum capacitive load at high speed operation :
1000 pF

d) Output impedance (approximate values)

| D.C. (resistive) load : | AC (capacitive) load : |
|---|---|
| at "0" level ) | 2000 Ω for positive going step |
| at "1" level ) < 0.03 Zg | < 0.03 Zg for negative going step |

(Zg is the generator impedance of the driving unit.)

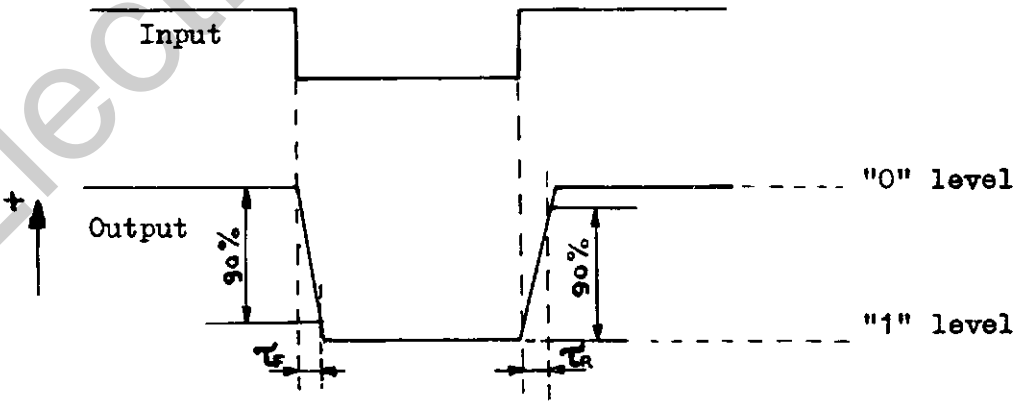
INPUT CHARACTERISTICS

| | |
|---|---|
| D.C. input : | applied to $W_1$ and $W_2$ |
| Necessary maximum amplitude : | 0.8 Em V |
| Permissible maximum amplitude : | Em V |
| Necessary maximum input current : | - 0.4 mA |
| Permissible maximum positive voltage : | 10 V |
| Permissible maximum input noise : | ± 1 V. |
| Input capacitance : | about 20 pF. |

SWITCHING TIMES

Input signal : negative going voltage step.
At the outputs $Q_1$ and $Q_2$ unloaded:
Fall time, $\tau_F$ < 0.1 μsec.
Rise time, $\tau_R$ < 0.1 μsec.

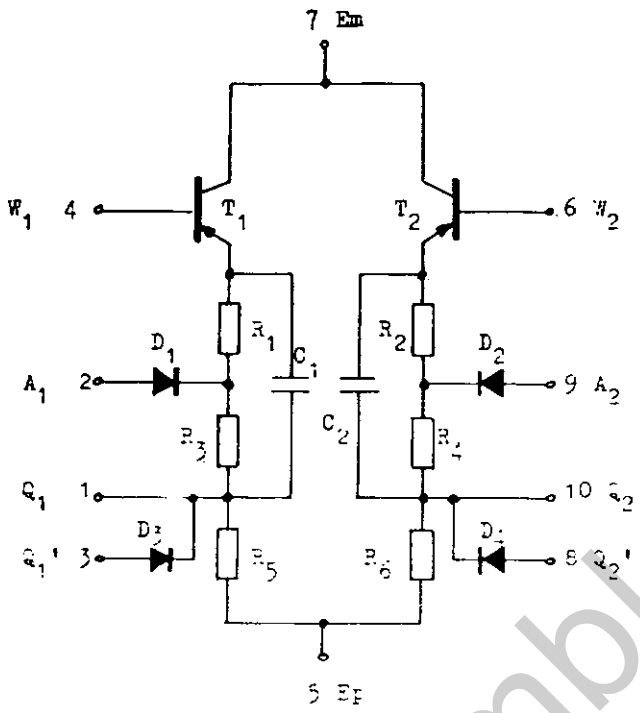
Explanation of these notations.

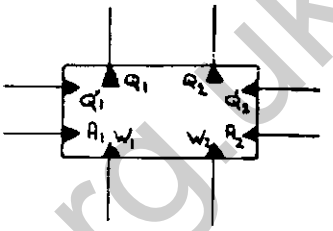



FREQUENCY RANGE: 0 - 100 kc/s

# TWIN EMITTER FOLLOWER 2EF2

2P 727 27
B8 940 03



TERMINAL INDICATION

Pin

1 = $Q_1$ = Direct output 1

2 = $A_1$ = Terminal of the clamping diode. To avoid hole storage effects connect $A_1$ to the collector output of the stage driven.

3 = $Q_1'$ = Output 1', drives only in one direction, to set or reset a flip-flop at its D.C. inputs.

4 = $W_1$ = Input 1

5 = Ep = Positive supply terminal (+ 6V)

6 = $W_2$ = Input 2

7 = Em = Negative supply terminal (-6V)

8 = $Q_2'$ = Output 2', drives only in one direction, to set or reset a flip-flop at its D.C. inputs.

9 = $A_2$ = Terminal of the clamping diode. To avoid hole storage effects connect $A_2$ to the collector output of the stage driven.

10 = $Q_2$ = Direct output 2





MULLARD EQUIPMENT LIMITED
A COMPANY OF THE MULLARD GROUP

## POWER REQUIREMENTS

Pin 5 Ep = + 6 V ± 10% 2 x (2-6) mA
Pin 7 Em = - 6 V ± 10% 2 x (2-6) mA
Deviations given are permitted in all combinations.

## OUTPUT CHARACTERISTICS

a) Output levels (at full load)
binary "0" > /+0·2/V
binary "1" < /-0·3/V

b) Available output currents:

| | at $Q_1$ and $Q_2$ | at $Q_1'$ and $Q_2'$ |
|---|---|---|
| at "0" level: | -1·5 mA | - |
| at "1" level: | +1·2 mA | +0·6 mA |

## INPUT CHARACTERISTICS

D.C. input: negative going voltage level applied to $W_1$ or $W_2$

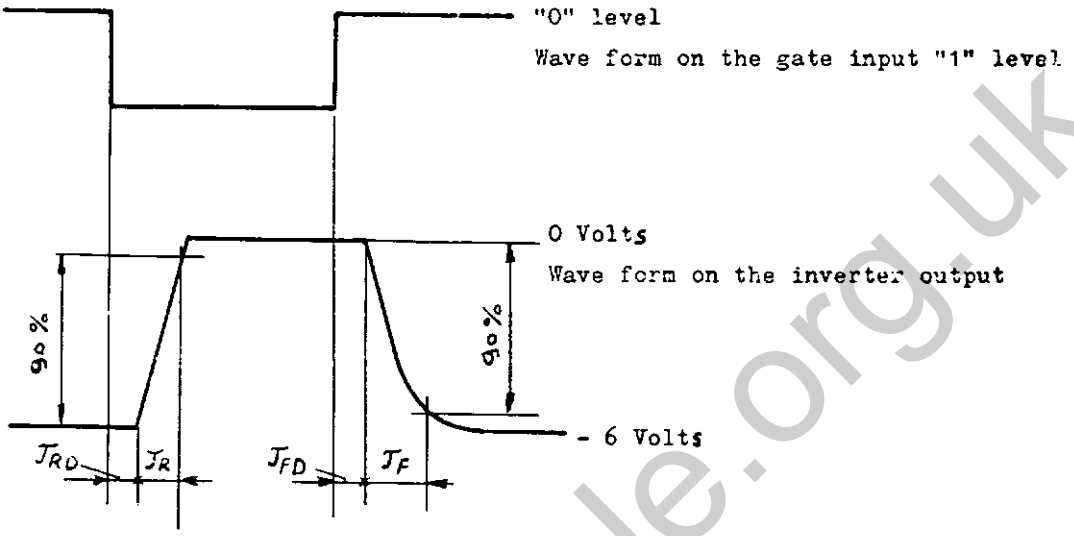
| | | |
|---|---|---|
| Necessary maximum amplitude: | | 0·7 Em V |
| Permissible maximum amplitude: | | Em V |
| Necessary maximum input current: | | -0·15 mA |
| Permissible maximum positive voltage: | | 10 V |
| Input capacitance: | approximately | 50 pF |

## SWITCHING TIMES

The output signal of this emitter follower unit will be exclusively used to drive a following grounded emitter stage. The switching times of a standard grounded emitter stage are given below at output currents of 0mA and -40mA respectively when driven by this emitter follower stage, which in turn is driven by an AND-gate followed by an OR-gate (collector of the driven transistor connected to A of EF2).

| | $I_Q$ = 0 mA | $I_Q$ = -40 mA |
|---|---|---|
| Rise delay time, $\tau_{RD}$ | < 0·3 μsec | < 0·3 μsec |
| Rise time, $\tau_R$ | < 0.3 μsec | < 1·5 μsec |
| Fall delay time, $\tau_{FD}$ | < 2·0 μsec | < 1·5 μsec |
| Fall time, $\tau_F$ | < 0·5 μsec | < 1·2 μsec |

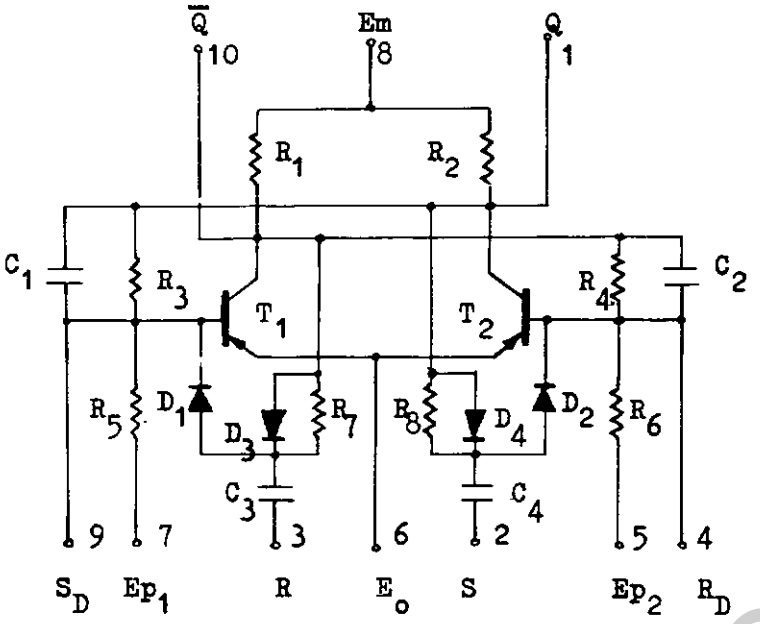
Explanation of the notations:

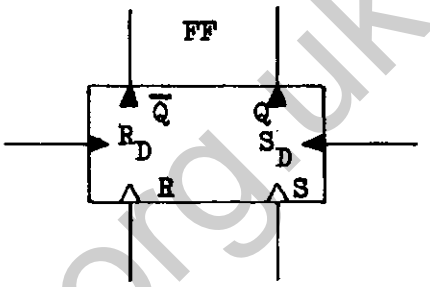



Frequency range: 0 - 100 kc/s

# FLIP - FLOP FF1

B8 920 00
B1 649 02




TERMINAL INDICATIONS

| Pin | | | | |
|---|---|---|---|---|
| 1 | = Q | = | Direct output | |
| 2 | = S | = | Set AC input | |
| 3 | = R | = | Reset AC input | |
| 4 | = $R_D$ | = | Reset DC input | |
| 5 | = $Ep_2$ | = | Positive supply terminal | (+ 6 V) |
| 6 | = Eo | = | Common " | ( 0 V) |
| 7 | = $Ep_1$ | = | Positive " | (+ 6 V) |
| 8 | = Em | = | Negative " | (- 6 V) |
| 9 | = $S_D$ | = | Set DC input | |
| 10 | = $\overline{Q}$ | = | Inverted output | |

POWER REQUIREMENTS

| | | | | |
|---|---|---|---|---|
| Pin 6 | Eo | = | 0 V | |
| Pin 8 | Em | = | - 6 V ± 10 % | 6 mA |
| Pin 5,7 | Ep | = | + 6 V + 10 % | 2 x 0.15 mA |

Deviations given are permitted in all combinations.

OUTPUT CHARACTERISTICS (Q and $\overline{Q}$ terminals)

a) Output levels (at full load)
binary "0" $< |-0.2|$ V
binary "1" $> |0.7\ Em|$ V

b) Permissible maximum load currents :
at "0" level : - 2.5 mA
at "1" level : + 0.5 mA
for both outputs simultaneously





MULLARD EQUIPMENT LIMITED
A COMPANY OF THE MULLARD GROUP

c) Typical maximum capacitive load at high speed operation:
2000 pF.

d) Output impedance (approximate values).

| D.C. (resistive) load : | | A.C. (capacitive) load : |
|---|---|---|
| at "0" level : | 50 Ω | 100 Ω for positive going step |
| at "1" level : | 1000 Ω | 1000 Ω for negative going stop |

INPUT CHARACTERISTICS

a) A.C. inputs : positive going voltage edge applied to S or R: to the interconnected terminals S and R (binary stage connection).

Permissible maximum rise time of the driving voltage edge : p.4 µsec.

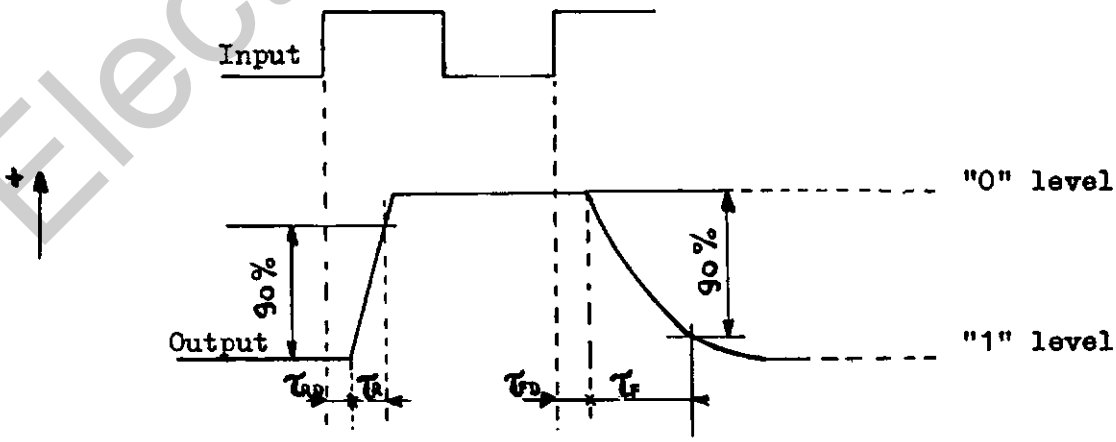
Necessary maximum amplitude : 0.7 Em V (typical 3 V).
Permissible maximum amplitude : Em V.
Minimum length of the driving pulse : 0.5 µsec.
Input impedance : equivalent to a capacity of about 500 pF.
Permissible maximum input noise : +1 V.

b) D.C. inputs : D.C. voltage level, applied to $S_D$ or $R_D$.
(in some applications it is necessary to use a series diode on these inputs to avoid unwanted loading of the flip-flop by the driving source).

Necessary maximum input current : -0.4 mA.
+1.0 mA.
Permissible maximum input current : -5 mA.
Permissible maximum positive input voltage : 10 V .
Static input resistance : about 800 Ω .

SWITCHING TIMES:
at the Q or $\bar{Q}$ outputs unloaded:

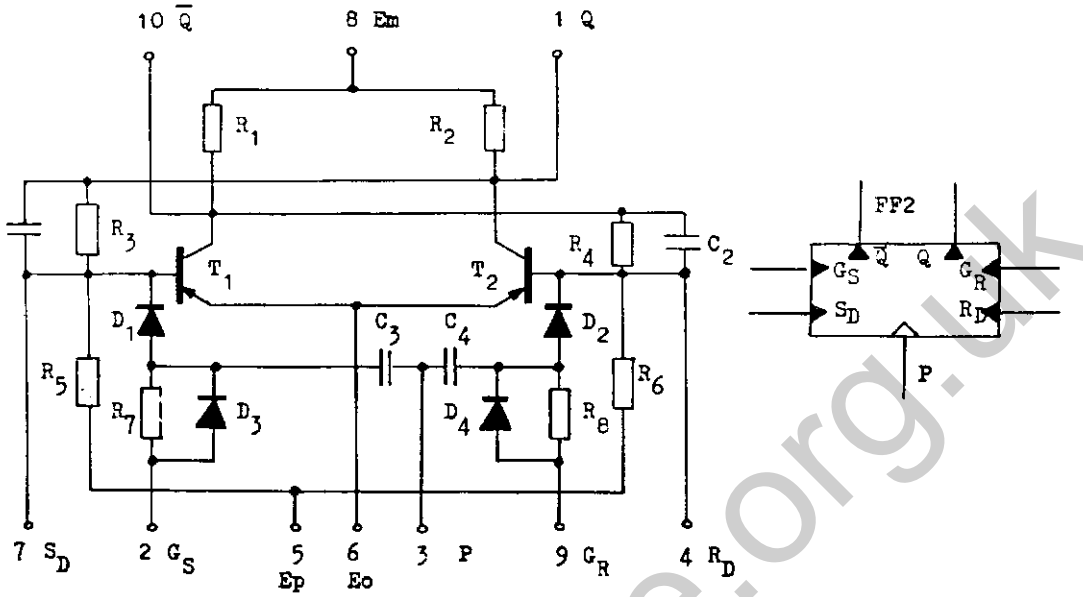
Rise time, $\tau_R$ < 0.3 µsec.
Rise delay time, $\tau_{RD}$ < 0.8 µsec.
Fall time, $\tau_F$ < 2 µsec.
Fall delay time, $\tau_{FD}$ < 0.6 µsec.




FREQUENCY RANGE: 0 - 100 kc/s

# FLIP FLOP FF2

2P 727 07
B8 920 01




## TERMINAL INDICATION

Pin

1 = Q = Direct output

2 = $G_s$ = Gate signal input. Connect to the direct output (Q) of the shift register flip-flop which lies opposite to the shifting direction desired.

3 = W = A.C. shift input. Connect parallel in the chain.

4 = $R_D$ = Reset DC input

5 = Ep = Positive supply terminal (+ 6V)

6 = $E_O$ = Common supply terminal (0 V)

7 = $S_D$ = Set DC input

8 = Em = Negative supply terminal (- 6V)

9 = $G_R$ = Gate signal input. Connect to the inverted output ($\overline{Q}$) of the shift register flip-flop which lies opposite to the shifting direction desired.

10 = $\overline{Q}$ = Inverted output.

## POWER REQUIREMENTS

Pin 6 Eo = 0 V
Pin 8 Em = - 6 V ± 10% 6 mA
Pin 5 Ep = + 6 V ± 10% 0·3 mA

Deviations given are permitted in all combinations.





MULLARD EQUIPMENT LIMITED
A COMPANY OF THE MULLARD GROUP

OUTPUT CHARACTERISTICS
(Q and $\overline{Q}$ terminals)

a) Output levels (at full load)
binary "0" < /-0·2/V
binary "1" > /0·7Em/V

b) Permissible maximum load currents:
at "0" level - 2·5 mA
at "1" level + 0·5 mA
for both outputs simultaneously

c) Typical maximum capacitive load
at high speed operation: 500pF

d) Output impedance (approximate values)

| D.C. (resistive) load: | | A.C. (capacitive) load: | |
|---|---|---|---|
| at "0" level: | 50 Ω | 100 Ω | for positive going step |
| at "1" level: | 1000 Ω | 1000 Ω | for negative going step |

INPUT CHARACTERISTICS

a) A.C. shift input: positive going voltage edge applied to P.

| | |
|---|---|
| Permissible maximum rise time of the driving voltage edge: | 0·4 μsec |
| Necessary maximum amplitude: 0·7EmV (typical: 3V) | |
| Permissible maximum amplitude: | Em V |
| Optimum shift pulse length for marginal circumstances and noise-free output waveform: | 2 μsec |
| Minimum shift pulse length: | 0·5 μsec |
| Input impedance: equivalent to a capacity of about 500pF | |
| Permissible maximum input noise level: | +1 V |

b) D.C. inputs: D.C. voltage level, applied to $S_D$ or $R_D$

| | | |
|---|---|---|
| Necessary maximum input current: | | |
| driven by a negative voltage level | | -0·4 mA |
| driven by a positive voltage level | | +1·0 mA |
| Permissible maximum input current: | | -5 mA |
| Permissible maximum input voltage: | | +10 V |
| Static input resistance: | approximately | 800Ω |

c) D.C. gate signal inputs: D.C. complement signals applied to GS and $G_R$

Necessary input amplitude is given by the general definition of binary levels.

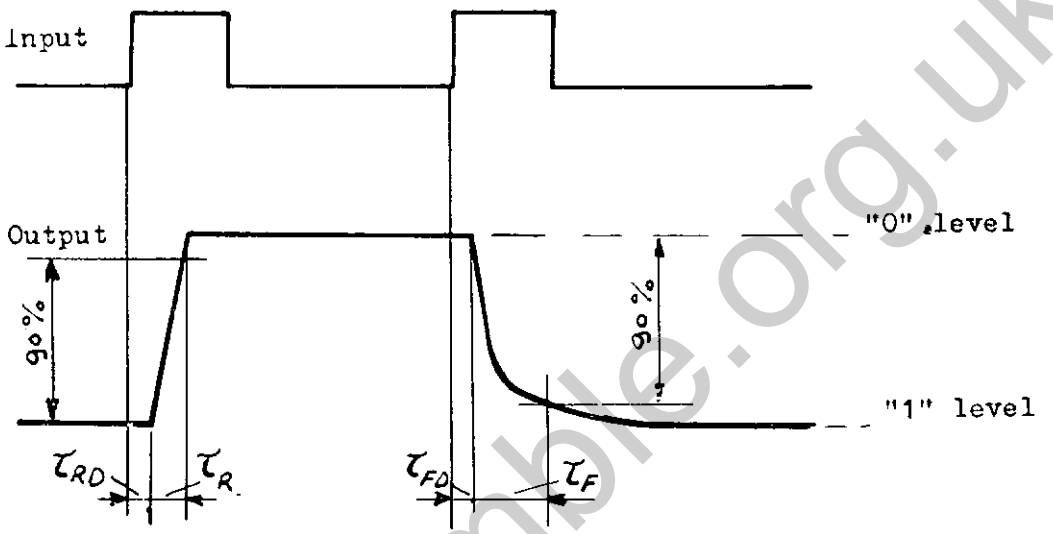
Note: The "0" level opens the gate

Input impedance: 5·6 kΩ in series with 560 pF

SWITCHING TIMES: at the Q or $\overline{Q}$ outputs (unloaded)

| | |
|---|---|
| Rise time, $\tau_R$ | < 0·3 μsec |
| Rise delay time, $\tau_{RD}$ | < 0·8 μsec |
| Fall time, $\tau_F$ | < 2 μsec |
| Fall delay time, $\tau_{FD}$ | < 0·6 μsec |

Explanation of these notations:




Frequency range: 0 - 100 kc/s

# FLIP-FLOP FF3

2P 727 82

COLOUR CODE: RED

## DATA SHEET

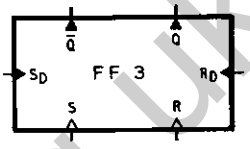
Unit FF3 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function when driven by means of a d.c. level or positive-going trigger signal. The unit can also be used as a binary scale-of-two with the trigger inputs interconnected.

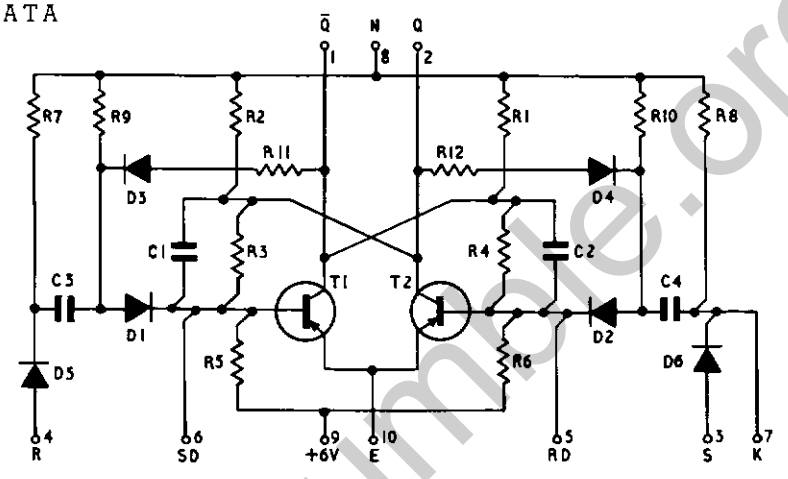
Frequency range : 0–100kc/s

Ambient temperature range : –20 to + 60°C

Weight : 20g approximately




CIRCUIT DATA




Terminal 1 = $\bar{Q}$ = output 1
2 = Q = output 2
3 = S = trigger input 2
4 = R = trigger input 1
5 = $R_D$ = d.c. input 2
6 = $S_D$ = d.c. input 1
7 = K = terminal for external trigger input
8 = N = supply –6V
9 = supply +6V
10 = E = common supply 0V

Power Supply

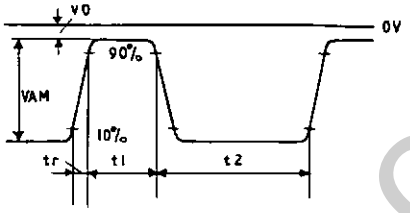
Terminal 8 : $V_N$ = –6V ± 5%, $-I_N$ = 8.8mA ) Nominal value
9 : V = +6V ± 5%, I = 0.6mA ) of the current
10 : $V_E$ = 0V common

## INPUT DATA

### Input Signal Requirements

### Trigger Input Signal (S and R terminals)

A positive-going voltage step is applied to terminal S or R, or with binary scale-of-two applications, to both terminals interconnected. This voltage step drives transistor T1 (T2) into the non-conducting state. External diodes can be connected to terminal K (in the same direction as diode D6) to provide the pulse-gate corresponding with terminal R, with extra trigger inputs or condition inputs.




Voltage

$V_{AM}$ = −0.7 VN minimum
= − VN maximum

−Vo = 0V minimum
= 0.2V maximum

| | | S or R | S and R interconnected |
|---|---|---|---|
| Required direct current | $I_{AD}$ = | 0.88mA minimum | 1.75mA minimum |
| Required current during the transient | | | |
| averaged over 0.4μsec | $I_{AT}$ = | 5mA minimum | 6mA minimum |
| 0.7μsec | = | 4mA minimum | 4.5mA minimum |
| Rise time | $t_r$ = | 0.7μsec maximum | |
| Pulse duration | $t_1$ = | 1μsec minimum | |
| | $t_2$ = | 8μsec minimum | |
| Input noise level | $V_n$ = | 1V peak to peak maximum | |

### D.C. Input Signal ($S_D$ and $R_D$ terminals)

A d.c. voltage level is applied to terminal $S_D$ or $R_D$. A positive voltage drives transistor T1 (T2) into the non-conducting state and a negative voltage drives it into the conducting state.

Transistor conducting

Current limiting value $-I_{SD,RD}$ = 0.7mA minimum ($-V_{SD,RD}$ = 0.4V maximum)
= 15mA maximum

Transistor non-conducting

| | | |
|---|---|---|
| Voltage | $V_{SD,RD}$ | = 0.2V minimum |
| limiting value | | = 15V maximum |
| Current | $I_{SD,RD}$ | = 1mA minimum |

OUTPUT DATA

Voltages and currents

Transistor conducting

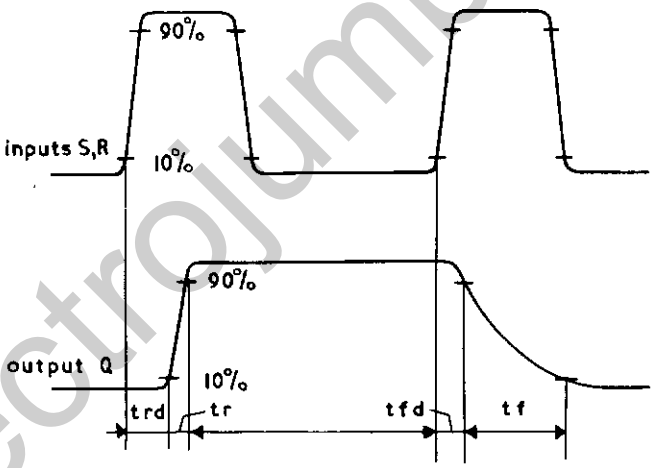
| | | |
|---|---|---|
| Voltage | $-V_Q$ | = −0.2V maximum |
| Available direct current | $I_{QD}$ | = 6mA maximum |
| Available current during the transient averaged over 0.4μsec | $-I_{QT}$ | = 11mA maximum |
| 0.7μsec | | = 14mA maximum |

Transistor non-conducting

| | | |
|---|---|---|
| Voltage | $-V_Q$ | = −0.7VN minimum |
| Available direct current | $-I_{QD}$ | = 0.7mA maximum |

Switching and delay times

This data is for guidance only and refers to an input signal as specified under INPUT DATA




| | | Unit unloaded | Unit loaded maximum |
|---|---|---|---|
| Rise delay | $t_{rd}$ | = 0.9μsec maximum | 1μsec maximum |
| Rise time | $t_r$ | = 0.3μsec maximum | 0.7μsec maximum |
| Fall delay | $t_{fd}$ | = 0.75μsec maximum | 0.8μsec maximum |
| Fall time | $t_f$ | = 1.5μsec maximum | 1.5μsec maximum |

# FLIP-FLOP FF4

2P 727 83

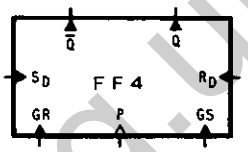
COLOUR CODE: RED

## DATA SHEET

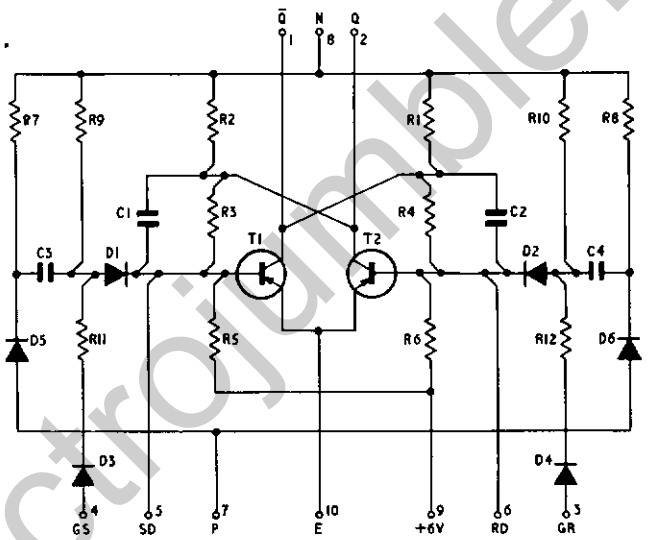
Unit FF4 contains a transistor bi-stable multivibrator circuit. The transistors are medium-speed switching types.

The circuit constitutes a memory function, when driven by means of a d.c. level or positive-going trigger signal. In the case of trigger drive, the switching of the flip-flop can be controlled by a d.c. level applied to the built-in gate circuits e.g. in shift registers.

| | | |
|---|---|---|
| Frequency range | : | see INPUT DATA |
| Ambient temperature range | : | −20 to +60°C |
| Weight | : | 20g approximately |




CIRCUIT DATA




Terminal 1 = $\bar{Q}$ = output 1
2 = Q = output 2
3 = $G_R$ = gate input 2
4 = $G_S$ = gate input 1
5 = $S_D$ = d.c. input 1
6 = $R_D$ = d.c. input 2
7 = P = trigger input
8 = N = supply −6V
9 = supply +6V
10 = E = common supply 0V

Power Supply

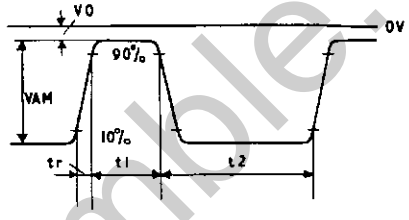
| | | | | | | |
|---|---|---|---|---|---|---|
| Terminal | 8 | : | $V_N$ = -6V ± 5%, | $-I_N$ = | 8.8mA ) | Nominal value |
| | 9 | : | = +6V ± 5%, | I = | 0.6mA ) | of the current |
| | 10 | : | $V_E$ = 0V common | | | |

INPUT DATA

Input Signal Requirements

Trigger Input Signal (P terminal)

A positive-going voltage step is applied to terminal P. This voltage step drives transistor T1 (T2) into the non-conducting state if the corresponding gate has been opened by an appropriate gate-input signal on terminal $G_R$ ($G_S$).




| | | | |
|---|---|---|---|
| Voltage | $V_{AM}$ = | -0.7 $V_N$ | minimum |
| | | - $-V_G$ | maximum |
| | $-V_o$ = | 0 V | minimum |
| | | 0.2V | maximum |
| Required direct current | $I_{AD}$ = | 1.75mA | minimum |
| Required current during the transient averaged over | | | |
| 0.4μsec | $I_{AT}$ = | 6 mA | minimum |
| 0.7μsec | | 4.5 mA | minimum |
| Rise time | $t_r$ = | 0.7μsec | maximum |
| Pulse duration | $t_1$ = | 3 μsec | minimum |
| | $t_2$ = | 11 μsec | minimum |
| Input noise level | $V_n$ = | 1V peak-to-peak | maximum |

D.C. Input Signal ($S_D$ and $R_D$ terminals)

A d.c. voltage level is applied to terminal $S_D$ or $R_D$. A positive voltage drives transistor T1 (T2) into the non-conducting state and a negative voltage drives it into the conducting state.

FF4 2 of 2.



Transistor conducting

| | | |
|---|---|---|
| Current | $-I_{SD,RD}$ = 0.7mA minimum | ($-V_{SD,RD}$ = 0.4V maximum) |
| limiting value | = 15 mA maximum | |

Transistor non-conducting

| | | |
|---|---|---|
| Voltage | $V_{SD,RD}$ = 0.2V minimum | |
| limiting value | = 15 V maximum | |
| Current | $I_{SD,RD}$ = 1mA minimum | |

Gate Input Signal ($G_S$, $G_R$ Terminals)

A d.c. voltage level is applied to terminal $G_R$ ($G_S$). Transistor T1 (T2) is driven into the non-conducting state by the trigger input signal (P terminal) if the corresponding gate is opened by an appropriate gate input signal.

| | | gate open | gate closed |
|---|---|---|---|
| Voltage | $-V_G$ = | 0V minimum | $-0.7V_N$ minimum |
| | | 0.2V maximum | $V_N$ maximum |
| Required direct current | $I_{GD}$ = | 1.75mA minimum | 1.2mA minimum |
| Required current during the transient | | to open gate | to close gate |
| averaged over 0.7μsec | $I_{GT}$ = | 1.6 mA minimum | – |
| Gate setting time | | | |
| when the gate input level changes at random: | $t_{GS}$ = | 17μsec minimum | 25μsec minimum |
| when the gate input level changes within 2μsec after the positive-going edge of the trigger signal: | $t_{GS}$ = | 11μsec minimum | 11μsec minimum |

Note: The latter applies to a shift-register configuration so that the maximum shift frequency is approximately 70kc/s.

During triggering, the G levels should not be at zero voltage level simultaneously.

The gate setting time is the required waiting time between the last G level change and the positive-going edge of the trigger pulse.

OUTPUT DATA

Voltages and currents

Transistor conducting

| | | |
|---|---|---|
| Voltage | $-V_Q$ = | 0.2V maximum |
| Available direct current | $-I_{QD}$ = | 6mA maximum |

Available current during the transient

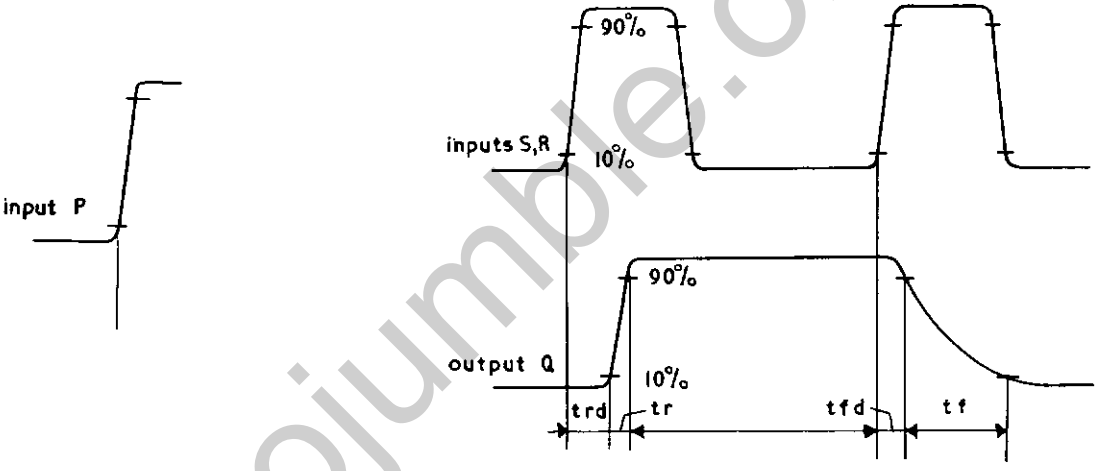
| averaged over | | | |
|---|---|---|---|
| 0.4μsec | $-I_{QT}$ | = 11mA | maximum |
| 0.7μsec | | = 14mA | maximum |

Transistor non-conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = $-0.7V_N$ | minimum |
| Available direct current | $I_{QD}$ | = 0.7mA | maximum |

Switching and delay times

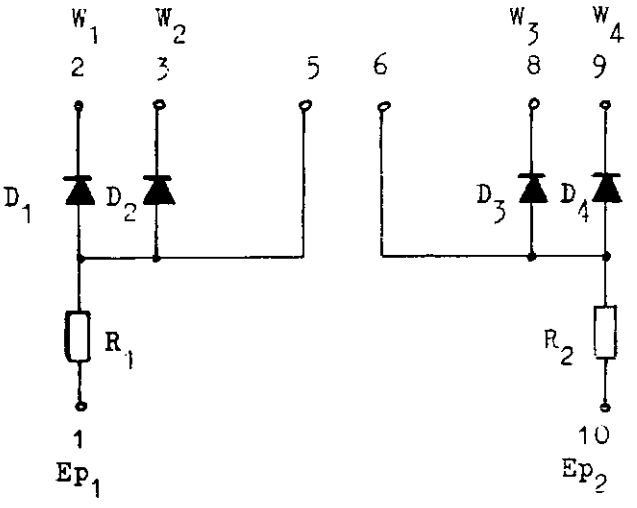
This data is for guidance only and refers to an input signal as specified under INPUT DATA.

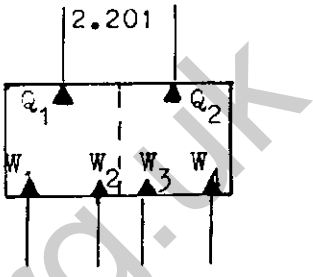



| | | Unit unloaded | Unit loaded maximum |
|---|---|---|---|
| Rise delay | $t_{rd}$ | = 0.9μsec maximum | 1μsec maximum |
| Rise time | $t_r$ | = 0.3μsec maximum | 0.7μsec maximum |
| Fall delay | $t_{fd}$ | = 0.75μsec maximum | 0.8μsec maximum |
| Fall time | $t_f$ | = 1.5μsec maximum | 1.5μsec maximum |

# TWIN OR GATE (2 x 2 INPUTS)

2P 727 30
B8 930 03




## TERMINAL INDICATION

Pin

1 = $Ep_1$ = Positive supply terminal (+ 6V)
2 = $W_1$ = Input 1
3 = $W_2$ = Input 2
4 = $W_3$ = n.c.
5 = $Q_1$ = Output 1
6 = $Q_2$ = Output 2
7 = $W_4$ = n.c.
8 = $W_5$ = Input 5
9 = $W_6$ = Input 6
10 = $Ep_2$ = Positive supply terminal (+ 6V).

## POWER REQUIREMENTS

Pin 1, 10 Ep = + 6 V ± 10% 2 × 0·06 mA

## OUTPUT CHARACTERISTICS

($Q_1$ and $Q_2$ terminals)

a) Output levels

binary "0" ) minimum 0·35 V more positive than the highest nega-
binary "1" ) tive input voltage level

b) Minimum available output currents:

at "0" level: -0·04 mA
at "1" level: determined by the driving circuit.

c) Output impedance: approximately equal to the output impedance of the driving circuit





MULLARD EQUIPMENT LIMITED
A COMPANY OF THE MULLARD GROUP

INPUT CHARACTERISTICS

D.C. input: negative voltage levels, applied to $W_1$ - $W_2$ or $W_3$ - $W_4$.

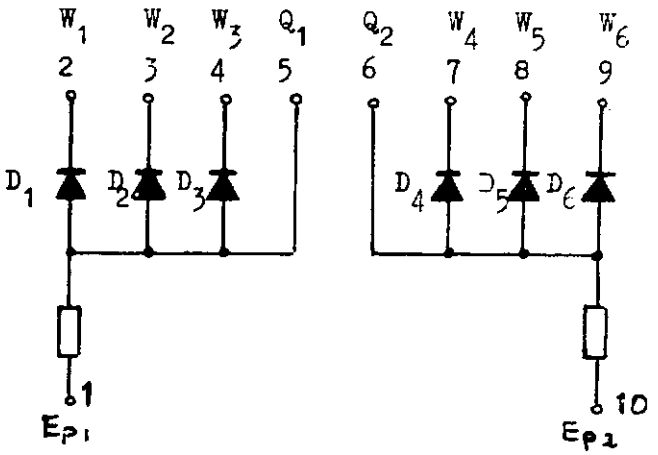
Input current:

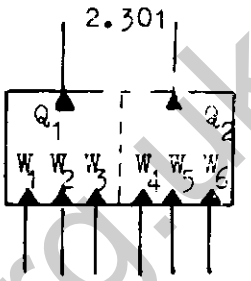
at "0" level maximum of -0·06 mA is distributed over the inputs as load for the driving stage.

at "1" level maximum of -0·08 mA will be lost from the driving current

# TWIN OR GATE (2 x 3 INPUTS)

2P 727 29
B8 930 02




## TERMINAL INDICATION

Pin

1 = $Ep_1$ = Positive supply terminal (+ 6V)
2 = $W_1$ = Input 1
3 = $W_2$ = Input 2
4 = $W_3$ = Input 3
5 = $Q_1$ = Output 1
6 = $Q_2$ = Output 2
7 = $W_4$ = Input 4
8 = $W_5$ = Input 5
9 = $W_6$ = Input 6
10 = $Ep_2$ = Positive supply terminal (+ 6V)

## POWER REQUIREMENTS

Pin 1, 10 Ep = + 6 V ± 10% 2 × 0·06 mA

## OUTPUT CHARACTERISTICS

($Q_1$ and $Q_2$ terminals)

a) Output levels

binary "0" ) minimum of 0·35 V more positive than the highest
binary "1" ) negative input voltage level.

b) Minimum available output currents:

at "0" level: -0·04 mA
at "1" level: determined by the driving circuit.

c) Output impedance:

approximately equal to the output impedance of the driving circuit.

## INPUT CHARACTERISTICS

D.C. Input: negative voltage levels, applied to $W_1$ - $W_3$ or $W_4$ - $W_6$.

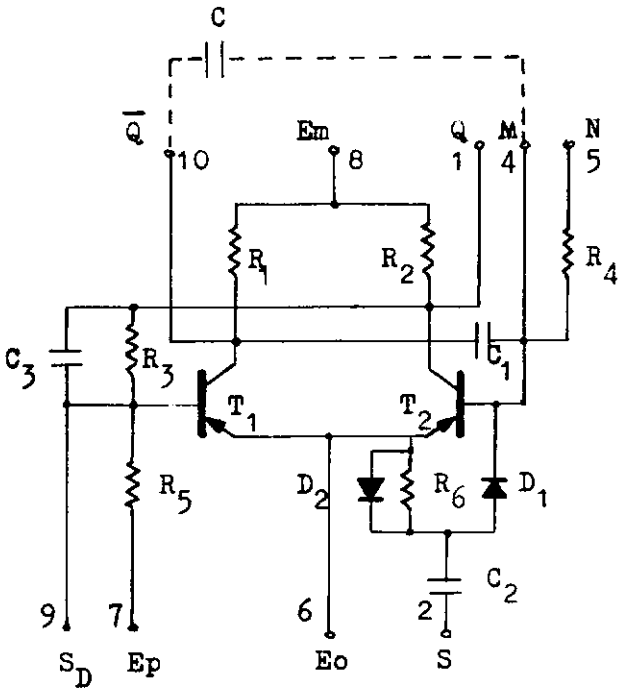
Input current:

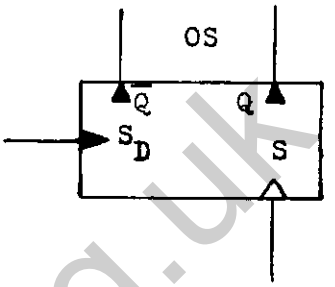
at "0" level: maximum of -0·06 mA is distributed over the inputs as load for the driving stage.

at "1" level: maximum of -0·08 mA will be lost from the driving current.

# ONE-SHOT MULTIVIBRATOR OS1

B8 950 01
B1 649 08




TERMINAL INDICATION

Pin

| | | | |
|---|---|---|---|
| 1 | = Q = | Direct output |
| 2 | = S = | A.C. input |
| 3 | = = | Internally connected with pin 4. |
| 4 | = M = | Terminal for external capacitance |
| 5 | = N = | To be connected to Em |
| 6 | = Eo = | Common supply terminal 0 V |
| 7 | = Ep = | Positive supply terminal + 6 V |
| 8 | = Em = | Negative supply terminal - 6 V |
| 9 | = $S_D$ = | (Normally not used) |
| 10 | = $\bar{Q}$ = | Inverted output |

POWER REQUIREMENTS

| | | | |
|---|---|---|---|
| Pin 6 | Eo | = | 0 V |
| Pins 5,8 | Em | = | - 6 V ± 10 % 6 mA |
| Pin 7 | Ep | = | + 6 V ± 10 % 0.15 mA |

Deviations given are permitted in all combinations.

OUTPUT CHARACTERISTICS

($Q$ and $\bar{Q}$ terminals)

a) Output levels (at full load)

| | | |
|---|---|---|
| binary "0" | < \|-0.2 \| | V |
| binary "1" | > \| 0.7 Em\| | V |

b) Permissible maximum load currents :

at "0" level : - 2.5 mA
at "1" level : + 0.5 mA
(for both outputs simultaneously)





MULLARD EQUIPMENT LIMITED
A COMPANY OF THE MULLARD GROUP

c) Typical maximum capacitive load at high speed operation :
2000 pF
This capacitive load increases the pulse length at the output Q:
< 25 %

d) Output impedance (approximate values)

| | D.C. (resistive) load : | A.C. (capacitive) load : |
|---|---|---|
| at "0" level : | 50 Ω | 100 Ω for positive going step |
| at "1" level : | 1000 Ω | 1000 Ω for negative going step |

INPUT CHARACTERISTICS

a) A.C. input : positive going voltage edge applied to S
Permissible maximum rise time of driving voltage edge :
0.4 µsec.

| | |
|---|---|
| Necessary maximum amplitude : | 0.7 Em V (typical:3V) |
| Permissable maximum amplitude : | 10 V |
| Minimum length of driving pulse : | 0.5 µsec. |
| Input impedance : equivalent to a capacity of about | 500 pF |
| Permissible maximum input noise : | + 1 V. |

b) D.C. input : normally not used.

SWITCHING TIMES

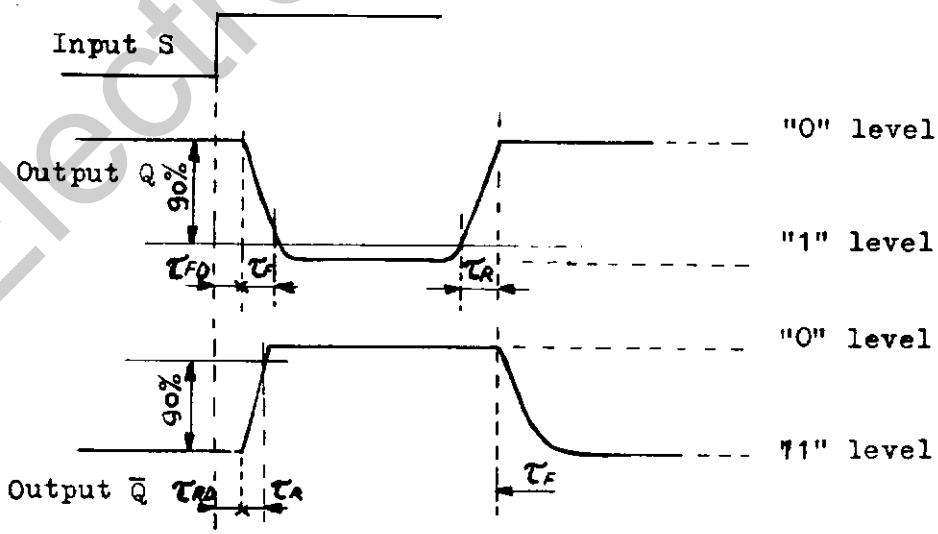
a) at the Q output, unloaded :

| | |
|---|---|
| Fall delay time, $\tau_{FD}$ | < 0.2 µsec. |
| Fall time, $\tau_F$ | < 1.8 µsec. |
| Rise time, $\tau_R$ | < 1 µsec. |

b) at the $\bar{Q}$ output, unloaded :

| | |
|---|---|
| Rise delay time, $\tau_{RD}$ | < 0.8 µsec. |
| Rise time, $\tau_R$ | < 0.3 µsec. |
| Fall time, $\tau_F$ | function of the C capacitance. |

c) Explanation of these notations



B8 950 01
B1 649 08

LENGTH OF THE OUTPUT PULSE:

The graph gives the output pulse length $\tau$, as a function of the C capacitance value, connected between pins : 4 and 10,
at ambient temperature : 25° C
at supply voltages : Em = - 6 V
Ep = + 6 V

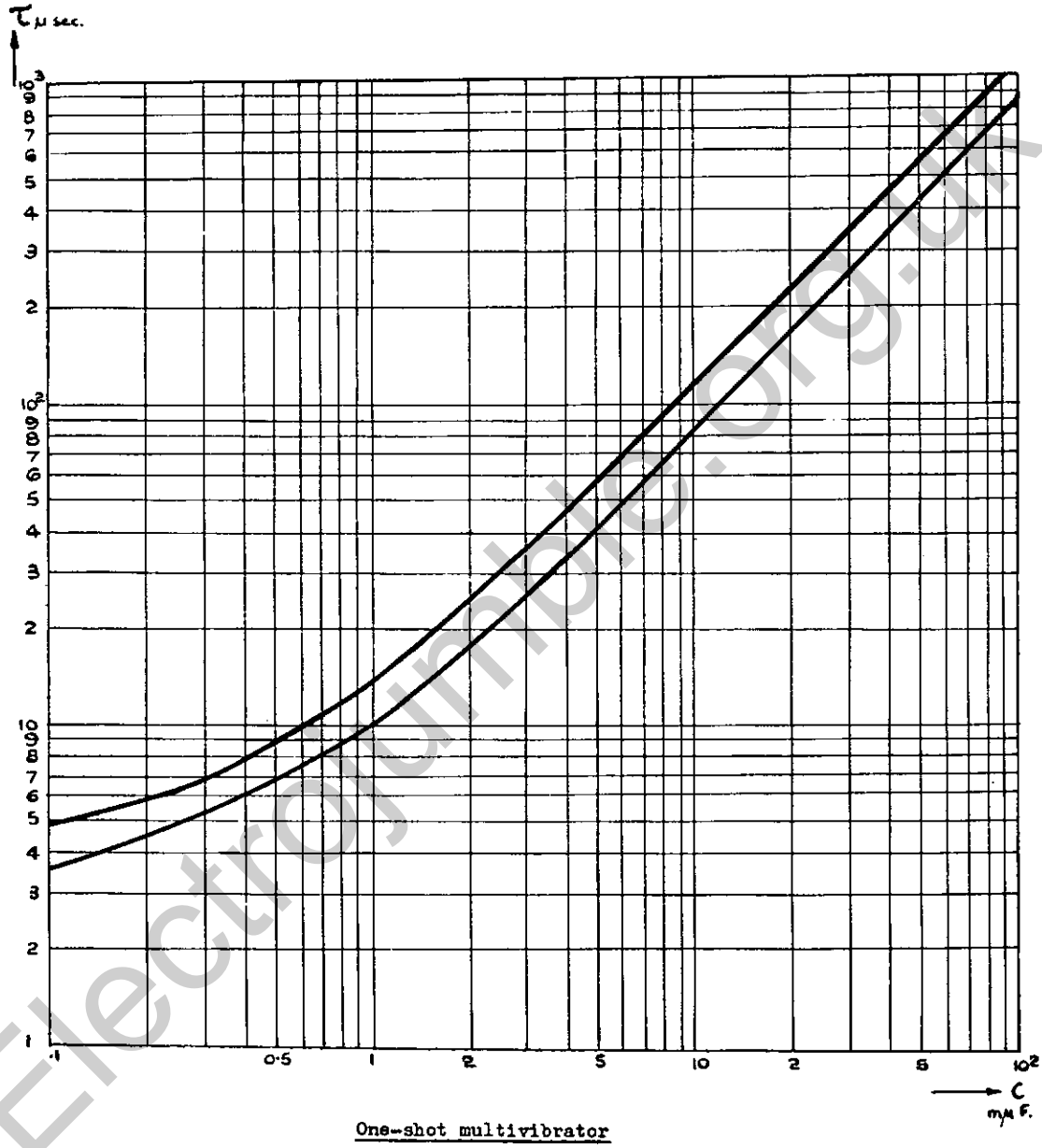
N.B. If an electrolytic capacitor is used for C, take care that the + terminal is connected to pin 4 of the OS. The use of electrolytic capacitors should be avoided, however, if narrow tolerances to the pulse length are given.

PULSE LENGTH STABILITY

a) an increase of the Em supply voltage of : 5 %
reduces the pulse length less than : 1 %
A change of the Ep supply voltage has practically no influence.

b) an increase of the ambient temperature of : 1°C
reduces the pulse length less than : 0.5 %

FREQUENCY RANGE : 0 - 100 kc/s




One-shot multivibrator

Output pulse length τ as a function of the external capacitance C.

# ONE-SHOT MULTIVIBRATOR OS2

2P 727 50

COLOUR CODE: GREEN

## DATA SHEET

Unit OS2 contains a transistorised monostable multivibrator circuit. The transistors are medium-speed switching types.

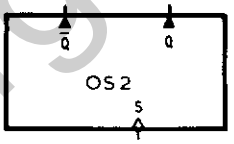
When a positive-going voltage step is applied to terminal S, the circuit generates a pulse at the Q terminals.

The duration of the output pulse is determined by the value of:

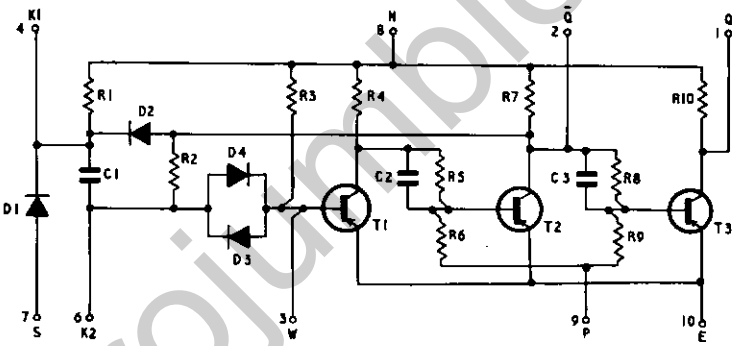
(a) The external capacitance, C, between terminals $K_1$ and $K_2$ (for pulses longer than the intrinsic value).

(b) The external resistance between the Q and W terminals (for pulses shorter than the intrinsic value).

| | | |
|---|---|---|
| Frequency range | : | 0–100kc/s |
| Ambient temperature range | : | −20 to + 60°C |
| Weight | : | 20g approximately |




CIRCUIT DATA




Terminal 1 = $\overline{Q}$ = output 1
2 = Q = output 2
3 = W = d.c. input
4 = $K_1$ = terminal for external capacitor
5 = not connected
6 = $K_2$ = terminal for external capacitor
7 = S = trigger input
8 = N = supply −6V
9 = P = supply +6V
10 = E = common supply 0V

Power Supply

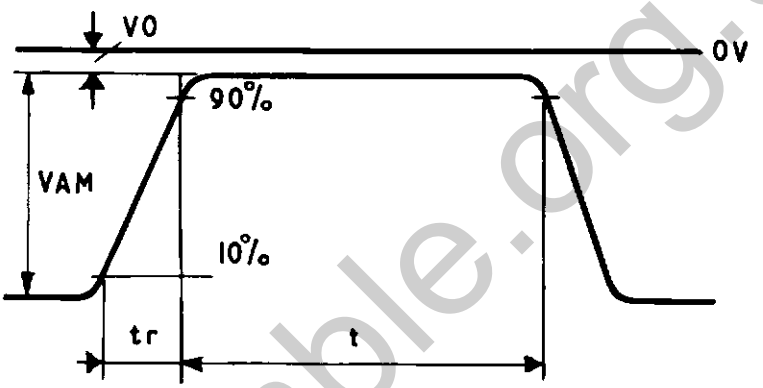
Terminal 8 = $V_N$ = −6V ± 5% $-I_N$ = 8.8mA ) Nominal value
9 = $V_p$ = +6V ± 5% $I_p$ = 0.4mA ) of the current
10 = $V_E$ = 0V common.

## INPUT DATA

### Input Signal Requirements

### Trigger Input signal (S terminal)

A positive-going voltage step is applied to terminal S. This voltage step drives transistor $T_2$ into the conducting and transistor $T_3$ into the non-conducting state.




| | |
|---|---|
| Voltage | $V_{AM}$ = $-0.7\,V_N$ minimum<br>= $-\,V_N$ maximum |
| | $-V_o$ = 0V minimum<br>= 0.2V maximum |
| Required direct current | $I_{AD}$ = 1.3mA minimum |
| Required current during the transient averaged over: 0.4μsec | $I_{AT}$ = 2.4mA minimum |
| 0.7μsec | 1.4mA minimum |
| Rise time without external capacitor: | $t_r$ = 0.4μsec maximum |
| with a capacitor of minimum 200pF between terminals $K_1$ and $K_2$: | $t_r$ = 0.7μsec maximum |
| Duration of driving pulse | t = 1μsec minimum |
| Recovery time | $t_{rec}$ = 6μsec minimum |
| when the duration of the output pulse ($t_o$) exceeds 7.5μsec: | $t_{rec}$ = 0.8 $t_o$ minimum |
| Input noise level | $V_n$ = 1V peak to peak maximum |

### D.C. Input signal (W terminal)

The W terminal is normally not used.

OSZ 2of2



## OUTPUT DATA

Voltages and currents

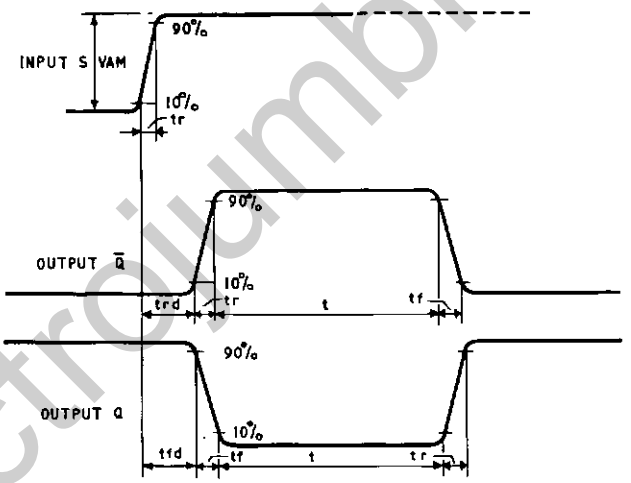
Transistor conducting

| | | Output Q | Output $\bar{Q}$ |
|---|---|---|---|
| Voltage: | $-V_Q$ = | 0.2V maximum | 0.2V maximum |
| Available direct current | $-I_{QD}$ = | 18mA maximum | 6mA maximum |
| Available current during the transient averaged over: 0.4µsec | $-I_{QT}$ = | 19mA maximum | 15mA maximum |
| 0.7µsec | = | 25mA maximum | 21mA maximum |

| Transistor non-conducting | | Output Q | Output $\bar{Q}$ |
|---|---|---|---|
| Voltage: | $-V_Q$ = | $-0.7V_N$ minimum | $-0.7V_N$ minimum |
| Available direct current: | $I_{QD}$ = | 0.7mA maximum | 0.3mA maximum |

Switching and delay times

This data is for guidance only and refers to an input signal, as specified under INPUT DATA.




| Unit unloaded | | Output Q | Output $\bar{Q}$ |
|---|---|---|---|
| Rise delay | $t_{rd}$ = | - | $t_{rS}$ +0.4µsec maximum |
| Rise time | $t_r$ = | 0.2µsec maximum | 0.2µsec maximum |
| Fall delay | $t_{fd}$ = $t_{rS}$ + | 0.5µsec maximum | - |
| Fall time | $t_f$ = | 0.4µsec maximum | 3µsec maximum |

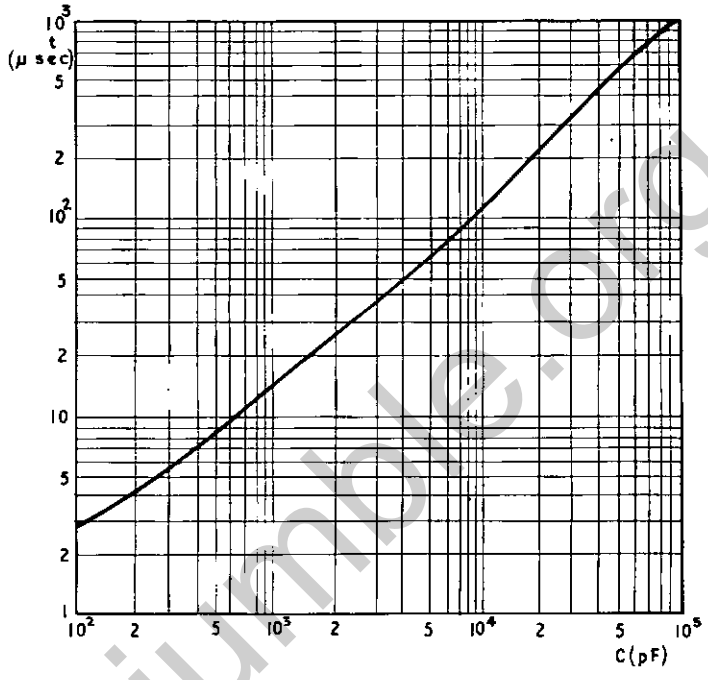
Duration of the output pulse

Unit unloaded

Intrinsic value: $t$ = 4µsec maximum

With resistor of 12kΩ
minimum between terminals Q and W: t = 2μsec maximum

With a capacitor between terminals $K_1$ and $K_2$, at an ambient temperature of 25°C, supply voltages $V_N$ = -6V and $V_p$ = +6V (refer to graph below).




Stability of pulse duration

An increase in supply voltage $V_N$ of 5%, increases the pulse duration by less than 1%. Any variation in supply voltage $V_p$ has practically no influence. An increase in ambient temperature of 1°C, reduces the pulse duration by less than 0.5%.

# POWER AMPLIFIER PA1

2 P 72755

## DATA SHEET

Power Amplifier PA1 consists of an n-p-n/p-n-p transistor amplifier circuit, designed to be used as a power amplifier in the circuit block range. The amplifier is non-inverting, and can be driven directly by circuit blocks FF1, FF2, FF3, FF4, 1A1 and 1A2.

The unit is capable of driving a load taking 600 mA at 60 V (absolute maximum values). The built-in diode across the output terminals, protects the output transistor from damage by voltage transients which occur when the unit is driving an inductive load.

The circuit is mounted on an epoxy-paper printed-wiring board, the output transistor being provided with an aluminium heat sink.

| | | |
|---|---|---|
| Frequency range | : | 0–100 c/s |
| Ambient temperature range | : | –20 to +60° C |
| Weight | : | 60 g (approximately) |

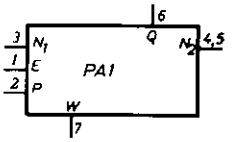



Fig. 1.

### CIRCUIT DATA

Terminal: 1 E = common supply 0 V
2 P = supply, +6 V
3 N1 = supply, –6 V
4 N2) = supply, maximum 60 V
5 N2) =
6 Q = output
7 W = input

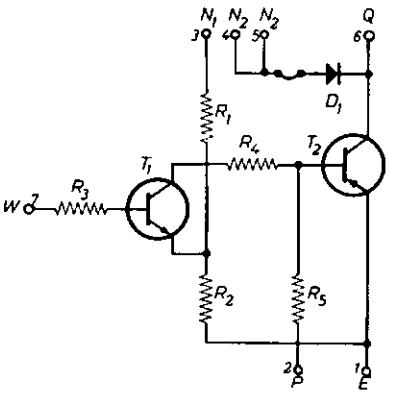



Fig. 2.

Power Supply

Terminal: 1 $V_E$ = 0 V common
2 $V_P$ = 6 V ± 10%, $I_P$ = max. 12.9 mA
3 $V_{N1}$ = –6 V ± 10%, $-I_{N1}$ = max. 70 mA
4) $V_{N2}$ = max. 60 V, $-I_{N2}$ = max. 600 mA
5)

MULLARD EQUIPMENT LIMITED

## INPUT DATA

Input Signal Requirements[+]

A d.c. voltage level is applied to terminal W.

Output transistor conducting:

| | | | |
|---|---|---|---|
| Voltage | $-V_w$ | = | max. 0.2V<br>min. 0V |
| Current | $I_w$ | = | min. 2.5mA |

Output transistor non-conducting:

| | | | |
|---|---|---|---|
| Voltage | $-V_w$ | = | min. 4.25V |
| Limiting value | | = | max. 13.2V |
| Current | $-I_w$ | = | min. 0.1mA |

## OUTPUT DATA

Output Signal Characteristics[+]

Output transistor conducting:

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = | max. 0.8V |
| Load current | $-I_Q$ | = | max. 600mA |

Output transistor non-conducting:

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = | max. 60V (dependent on the value of $V_{N2}$ which is 60V absolute maximum). |
| Leakage current | $-I_Q$ | = | max. 12mA |

Switching and Delay Times (for guidance only)

A square-wave input signal is applied with an amplitude of 4.25V, a rise time of 1$\mu$ sec and a fall time of 2$\mu$ sec.

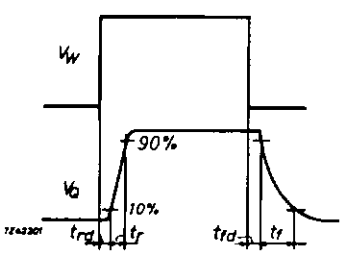



Fig. 3.

[+]This data applies to the most adverse working conditions for a combination of units, namely to supply voltages $V_N$ = -5.4V and $V_P$ = +6.6V. Unless stated to the contrary, all voltage and current figures quoted, represent absolute maximum values.

Unit loaded with a 100-ohm resistor

| | | | |
|---|---|---|---|
| Rise delay | $t_{rd}$ | = | max. 15$\mu$ sec |
| Rise time | $t_r$ | = | max.120$\mu$ sec |
| Fall delay | $t_{fd}$ | = | max. 90$\mu$ sec |
| Fall time | $t_f$ | = | max.110$\mu$ sec |

Unit loaded with an inductive load

The unit is provided with a built-in diode to protect the output transistor from damage by voltage transients which occur when an inductive load is switched. This protection is achieved at the expense of a very long, fall delay time of the load current. At supply voltages below 60V, however, a jumper wire in series with the diode can be interchanged with a resistor to decrease the delay time. The maximum permissible value of this resistor is given in the graph below, with current flowing through the load at the moment of switching-off as a parameter.

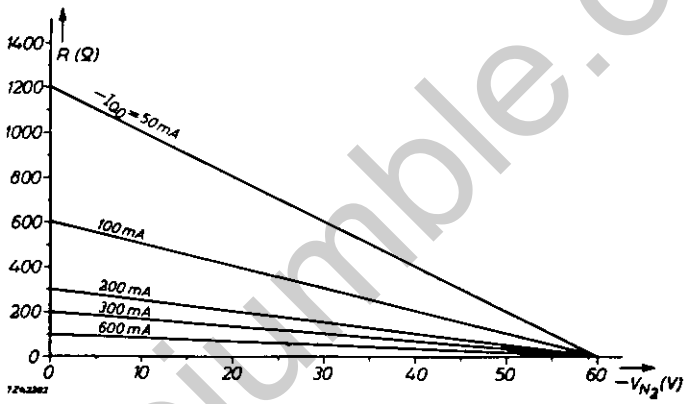



Fig. 4.

MECHANICAL CONSTRUCTION

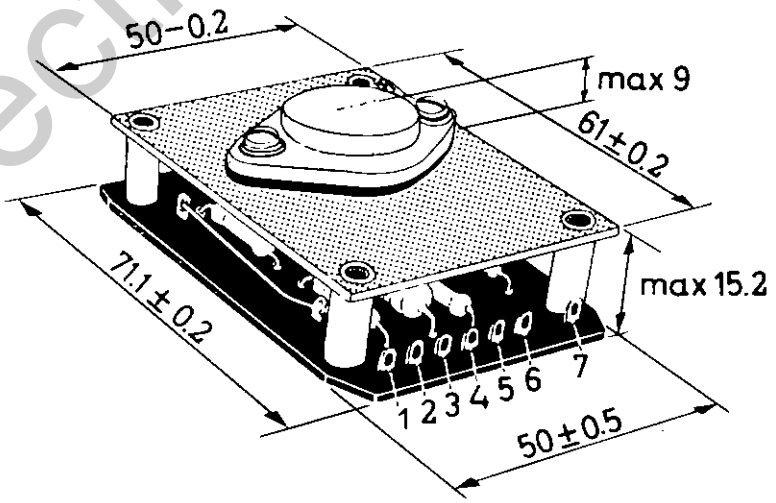



Fig. 5.

The dimensions (approximately 71mm x 50mm x 25mm) and terminal location can be seen in Fig.5. Since the aluminium heat sink is insulated from the circuit, no special measures need be taken with regard to mounting the unit.

## MOUNTING INSTRUCTIONS

The mechanical design of the PA1 is based on its use in standardised mounting chassis B8 716 09 or B8 716 10. To facilitate mounting, small mounting parts are supplied with the unit. The PA1 can, by means of these parts, be fastened directly into chassis type B8 716 09 for side-by-side mounting. In the chassis for circuit blocks mounted on printed-wiring boards, the same parts are used as a stand-off. Up to four Power Amplifiers PA1 can be mounted on a standard printed-wiring board (approximately 122mm x 180mm); because of the combined dimensions of the Power Amplifiers and the printed-wiring board, a vacant position must be left in the mounting chassis between each printed-wiring board.

To ensure adequate cooling, the PA1 must be mounted in such a way that a free flow of air through it is guaranteed.

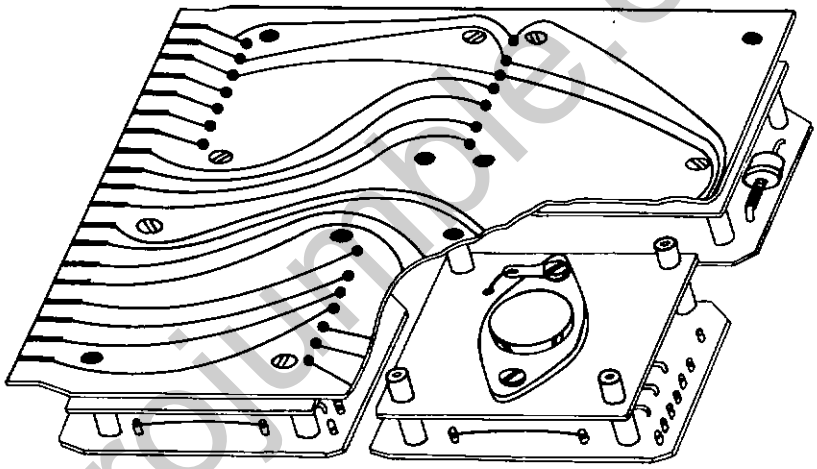


Fig. 6

For mounting in chassis B8 716 09, use is made of a metal bracket as shown in Fig.7. The PA1 occupies the width of 3 circuit blocks.

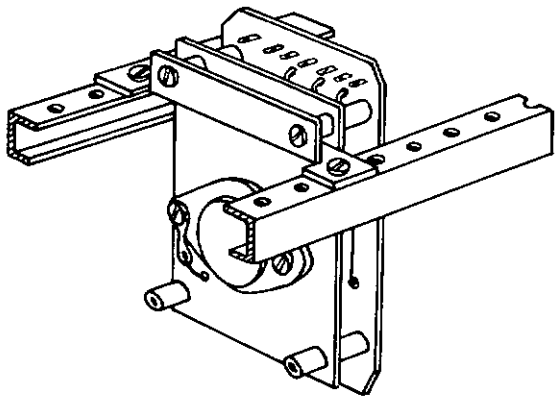


Fig. 7.

# PULSE GENERATOR PG1

**B 8 950 02**

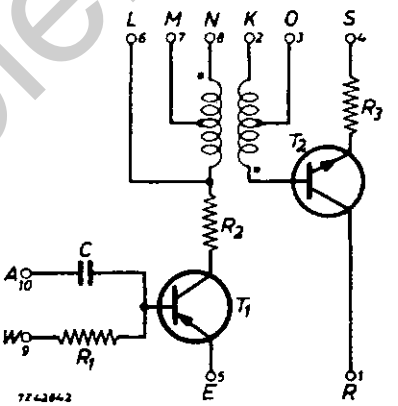
**COLOUR CODE: GREEN**

## DATA SHEET

The unit PG1 is designed to operate as a "short-interval" switch for the drive wires and the inhibit wires of a ferrite-core memory.

The switching of the n-p-n output transistor is controlled by an input level change applied to the pre-amplifier stage.


| | | | | |
|---|---|---|---|---|
| Terminal | 1 | = R | = | Switch in |
| | 2 | = K | = | Transformer terminal |
| | 3 | = O | = | Transformer terminal |
| | 4 | = S | = | Switch out |
| | 5 | = E | = | Common supply 0 V |
| | 6 | = L | = | Transformer terminal |
| | 7 | = M | = | Transformer terminal |
| | 8 | = N | = | Supply −6V |
| | 9 | = W | = | D.C. input |
| | 10 | = A | = | Trigger input |




Power Supply

Terminal 5 = $V_E$ = 0 V common

7 or 8 = $V_N$ = −6 V ± 2%, $-I_N$ = 50 mA (Nominal value)

APPLICATION DATA

The unit is normally used for ferrite-core memory operation in combination with other standard circuit blocks.

Input (A and W terminal)

The interconnected A and W terminal are normally driven by the Q output of an EF2 emitter follower.

A positive going input signal switches the output transistor into the conducting state.



MULLARD EQUIPMENT LIMITED

597-1-63

EF2 input signal requirements

| | | | |
|---|---|---|---|
| Voltage | $V_{WM}$ | = | min. 3.7 V |
| | | = | max. $V_N$ |
| Required current | $-I_W$ | = | min. 0.15 mA |
| Rise time | $t_r$ | = | max. 0.4 $\mu$sec |
| Fall time | $t_f$ | = | max. 0.4 $\mu$sec |

Output (R and S terminal)

The output terminals are connected in series with a group of drive wires via 2.SS1's or an inhibit wire.

Pulse Generator conducting

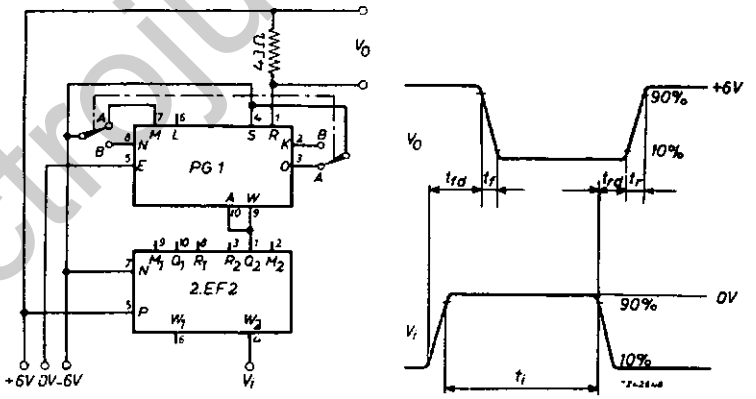
| | | | |
|---|---|---|---|
| Current | $I_{RS}$ | = | max. 250 mA |
| Voltage | $V_{RS}$ | = | max. 1.5 V peak value |

Pulse Generator non-conducting

| | | | |
|---|---|---|---|
| Current | $-I_{RS}$ | = | max. 2.5 mA at $V_{RS}$ = -15 V |

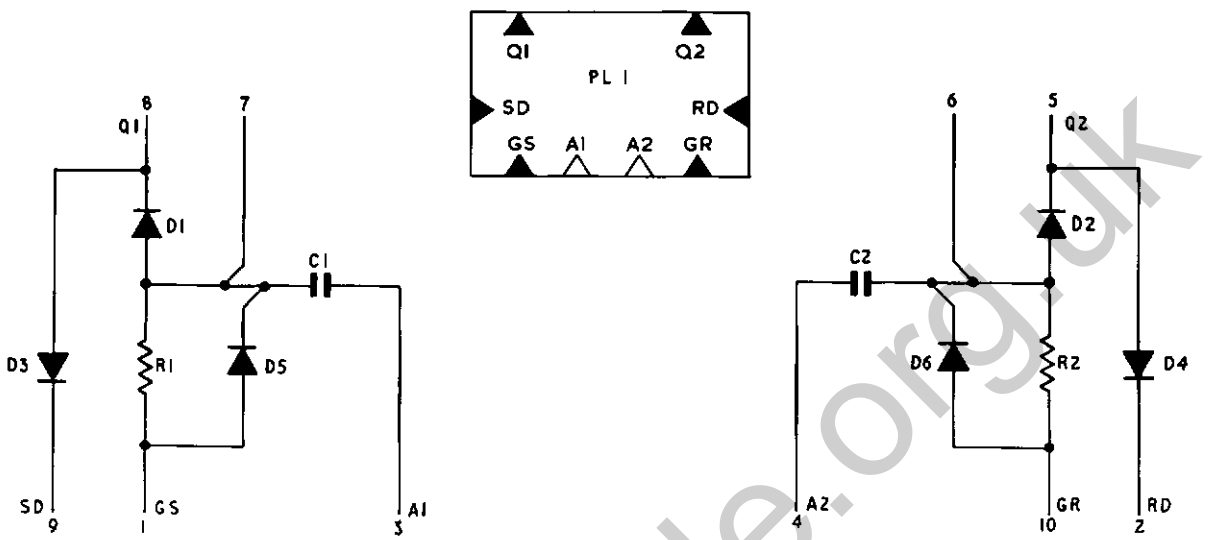
Switching and delay times

These data are for guidance only and refer to an input signal as specified under EF2 input signal requirements; they are measured in the circuit given below.




| Switch position | | | A | B |
|---|---|---|---|---|
| Input pulse duration | $t_i$ | = | 2 | 3.5 $\mu$sec |
| Repetition frequency | $f_i$ | = | 100 | 70 kc/s |
| Fall delay | $t_{fd}$ | = max. | 0.75 | 0.75 $\mu$sec |
| Fall time | $t_f$ | = max. | 0.45 | 0.45 $\mu$sec |
| Rise delay | $t_{rd}$ | = max. | 1 | 1.2 $\mu$sec |
| Rise time | $t_r$ | = max. | 0.25 | 0.25 $\mu$sec |

## DATA SHEET




TERMINAL INDICATION

PIN

1 = $G_S$ = Gate signal input. Connect to the direct output (Q) of the Flip Flop from which information is to be taken.

2 = $R_D$ = Reset d.c. input.

3 = $A_1$ = Pulse input 1.

4 = $A_2$ = Pulse input 2.

5 = $Q_2$ = Connect the reset d.c. input ($R_D$) of the Flip Flop.

6 = Not normally used.

7 = Not normally used.

8 = $Q_1$ = Connect to the set d.c. input (SD) of the Flip Flop.

9 = $S_D$ = Set d.c. input.

10 = $G_R$ = Gate Signal input. Connect to the inverted output (Q) of the Flip Flop from which information is to be taken.

The shift register Flip Flop and shift register logic combination has, besides the possibility of a two-directional shift, similar operation properties to the FF2 alone; therefore for further data refer to the FF2 sheets.

# TWIN PULSE LOGIC UNIT 2.PL2

2P 727 58

COLOUR CODE: ORANGE

## DATA SHEET

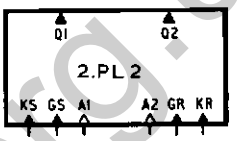
Unit 2.PL2 contains two identical pulse gates, which are controlled by a d.c. voltage level.

The circuits are used normally in conjunction with flip-flop circuits. With the twin-pulse logic unit, a second pair of a.c. inputs is provided for a flip-flop FF3; a bi-directional shift register can be constructed by combining with a flip-flop FF4. In these applications, the 2.PL2 output terminals are connected directly to the flip-flop d.c. input terminals.

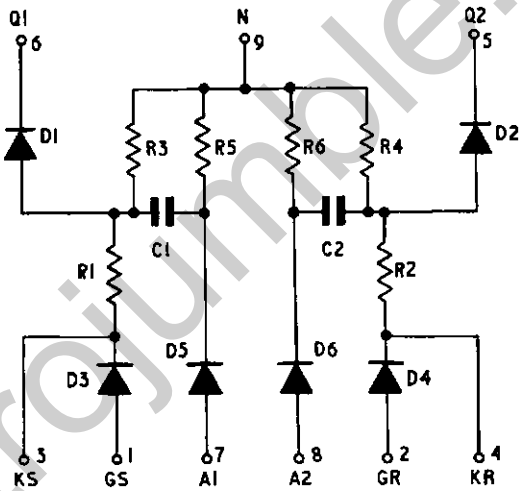
Frequency range: see INPUT DATA

Ambient temperature range: −20 to +60°C

Weight: 20 g approximately




CIRCUIT DATA




Terminal 1 = $G_S$ = gate input 1
2 = $G_R$ = gate input 2
3 = $K_S$ = terminal for external gate input
4 = $K_R$ = terminal for external gate input
5 = $Q_2$ = output 2
6 = $Q_1$ = output 1
7 = $A_1$ = trigger input 1
8 = $A_2$ = trigger input 2
9 = N = supply −6V
10 = not connected

Power Supply

Terminal 9 : $V_N$ = −6V ± 5%, $-I_N$ = 0–2.5mA Nominal value of the current.

INPUT DATA

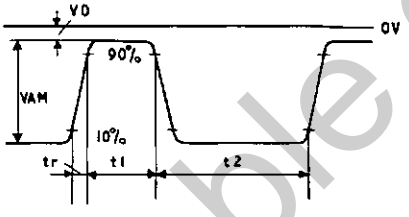
This data is dependent on the driven circuit; the values given apply to the twin pulse logic unit, when used in conjunction with flip-flops FF3 or FF4.

Input Signal Requirements

Trigger Input Signal (A terminals)

A positive-going voltage step is applied to terminal A1 or A2 or to both terminals interconnected.

This voltage step passes the pulse gate if the gate has been opened by an appropriate gate-input signal on terminal $G_S$ ($G_R$).




| | | | |
|---|---|---|---|
| Voltage | $V_{AM}$ | $= -0.7\,V_N$ | minimum |
| | | $= -\ V_G$ | maximum |
| | $-V_o$ | $= 0\,V$ | minimum |
| | | $= -0.2\,V$ | maximum |

| | | $A_1$ or $A_2$ | $A_1$ and $A_2$ interconnected |
|---|---|---|---|
| Required direct current: | $I_{AD}$ | $= 0.88$mA minimum | 1.75mA minimum |
| Required current during the transient averaged over | | | |
| 0.4$\mu$sec: | $I_{AT}$ | $=$ 5mA minimum | 6mA minimum |
| 0.7$\mu$sec: | | $=$ 4mA minimum | 4.5 mA minimum |
| Rise time: | $t_r$ | $= 0.7\mu$sec maximum | |
| Pulse duration: | $t_1$ | $= 3\mu$sec minimum | |
| | $t_2$ | $= 11\mu$sec minimum | |
| Input noise level: | $V_n$ | $= 1$V peak-to-peak maximum | |

Gate Input Signal (G terminals)

A d.c. voltage level is applied to terminal $G_S$ ($G_R$)

The trigger input signal, terminal $A_1$ ($A_2$), passes if the corresponding gate is opened by an appropriate gate-input signal.

External diodes can be connected to terminal $K_S$ ($K_R$) (in the same direction as diode $D_3$ ($D_4$), to provide the corresponding pulse gate with extra trigger inputs or condition inputs.

| | Gate open | Gate closed |
|---|---|---|
| Voltage: | $-V_G$ = 0V minimum | $-0.7V_N$ minimum |
| | = 0.2V maximum | $V_N$ maximum |
| Required direct current: | $I_{GD}$ = 1.75mA minimum | 1.2mA minimum |
| Required current during the transient: | To open gate | To close gate |
| averaged over 0.7$\mu$ sec: | $I_{GT}$ = 1.6mA minimum | |
| | To open gate | To close gate |
| Gate setting time | | |
| when the gate input level changes at random: | $t_{GS}$ = 17$\mu$sec minimum | 25$\mu$sec minimum |
| when the gate input level changes within 2$\mu$sec after the positive-going edge of the trigger signal: | $t_{GS}$ = 11$\mu$sec minimum | 11$\mu$sec minimum |

Notes:

(1) The latter applies to a shift-register configuration so that the maximum shift frequency is approximately 70kc/s.

(2) During triggering, the G levels should not be at zero voltage level simultaneously.

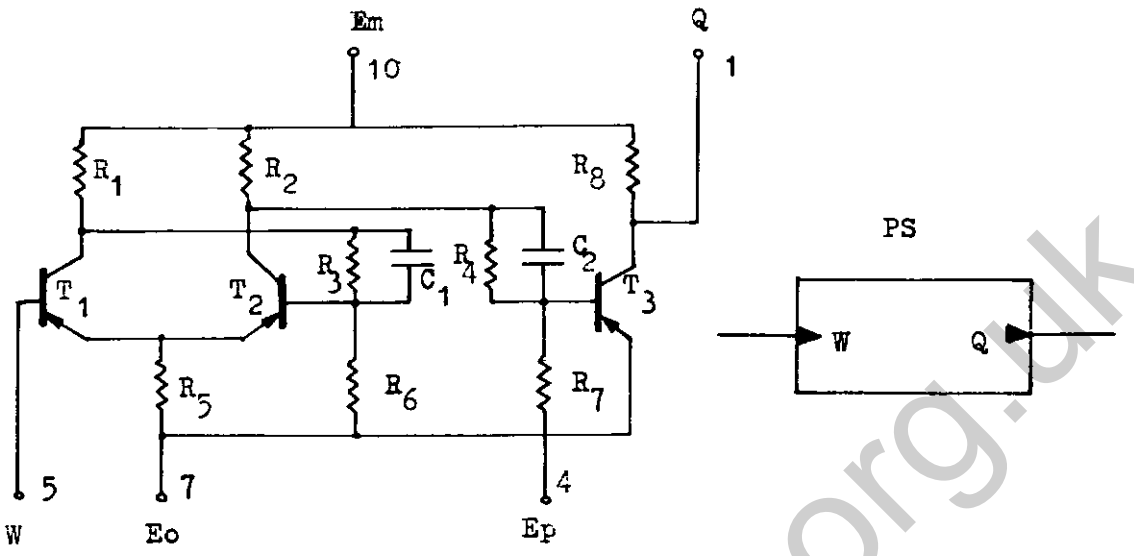
(3) The gate-setting time is the required waiting time between the last G level change and the positive-going edge of the trigger pulse.

OUTPUT DATA

When the unit is used in conjunction with flip-flops FF3 and FF4, the output terminals, $Q_1$ and $Q_2$, are directly connected to the flip-flop d.c. input terminals ($S_D$ and $R_D$).

# PULSE SHAPER PS1

B8 950 00
B1 649 01




## TERMINAL INDICATION

Pin

| | | | |
|---|---|---|---|
| 1 | = Q | = | Output |
| 4 | = Ep | = | Positive supply terminal (+ 6 V) |
| 5 | = W | = | Input |
| 7 | = Eo | = | Common supply terminal (0 V) |
| 10 | = Em | = | Negative supply terminal (- 6 V) |

Note: Pins 2, 3, 6, 8 and 9 are not present.

## POWER REQUIREMENTS

| | | | |
|---|---|---|---|
| Pin 7 | Eo | = 0 V | |
| Pin 10 | Em | = - 6 V ± 10 % | (3.8 - 6.8) mA |
| Pin 4 | Ep | = + 6 V ± 10 % | 0.27 mA |

Deviations given are permitted in all combinations.

## OUTPUT CHARACTERISTICS

(Q terminal)

a) Output levels (at full load) :

binary "0" $< |-0.2|$ V

binary "1" $> |0.7 \quad Em|$ V

b) Permissible load currents

at "0" level : - 1.2 mA

at "1" level : + 0.6 mA

c) Typical maximum capacitive load at high-speed operation :

1000 pF



MULLARD EQUIPMENT LIMITED
A COMPANY OF THE MULLARD GROUP

d) Output impedance (approximate values)

| | D.C. (resistive) load | A.C. (capacitive) load |
|---|---|---|
| at "0" level | 50 Ω | 100 Ω for positive going step |
| at "1" level | 2200 Ω | 2200 Ω for negative going step |

INPUT CHARACTERISTICS

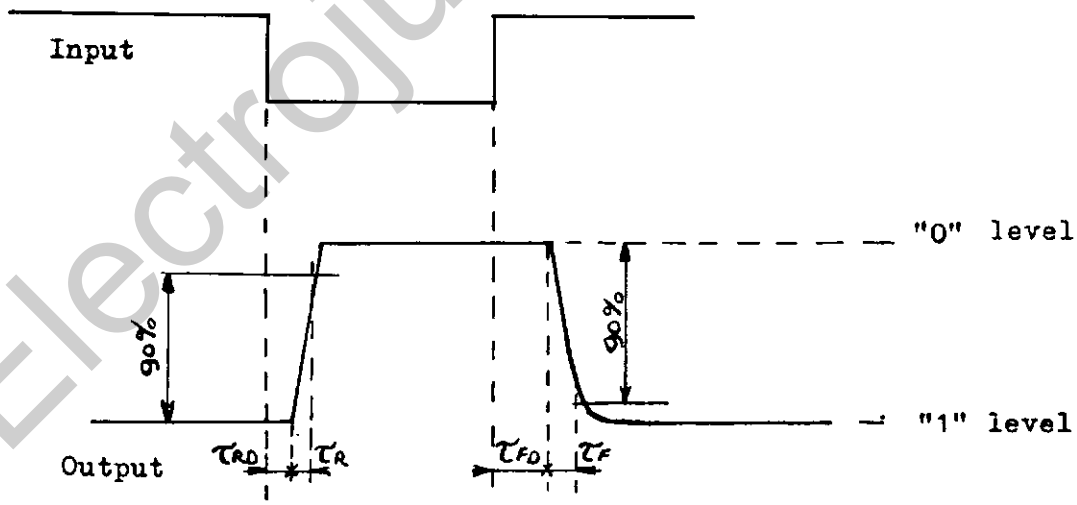
| | |
|---|---|
| D.C. input : | applied to W |
| Necessary maximum amplitude : | 0.4 Em V |
| Hysteresis : | < 0.4 Em V |
| Permissible maximum amplitude : | Em V |
| Necessary maximum input current : | - 0.1 mA |
| Input capacitance | about 20 pF |
| Permissible maximum positive voltage : | 10 V |
| Permissible maximum input noise : | - 1 V |

SWITCHING TIMES

Input signal : negative going voltage step
At the Q output, unloaded :

| | |
|---|---|
| Rise time, $\tau_R$ | 0.2 µsec |
| Rise delay time, $\tau_{RD}$ | 0.1 µsec |
| Fall time, $\tau_F$ | 0.2 µsec |
| Fall delay time, $\tau_{FD}$ | function of the driving current |

Explanation of the notations :




FREQUENCY RANGE : 0 - 100 kc/s

# READ AMPLIFIER RA1

2P 727 31

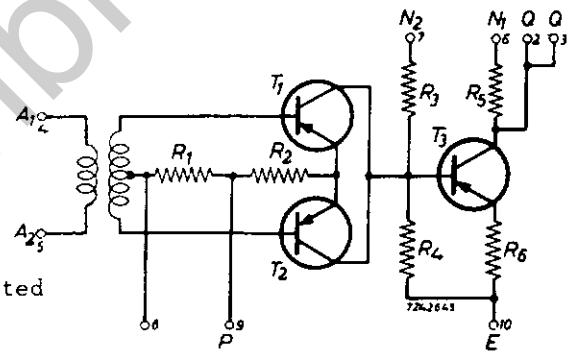
COLOUR CODE: YELLOW

## DATA SHEET

The unit RA1 is designed to amplify the signals originating from the sense wire of a small ferrite-core memory equipped with cores type 6B2, FX 2423 or equivalent types. The maximum plane size is 16 x 16 cores.

The circuit consists of a two stage amplifier; the first stage is balanced, so that the circuit can deal with either positive going or negative going input signals.


| | | | | |
|---|---|---|---|---|
| Terminal | 1 | = | | not connected |
| | 2 | = | | |
| | 3 | = | Q | = output |
| | 4 | = | $A_1$ | = input |
| | 5 | = | $A_2$ | |
| | 6 | = | $N_1$ | = supply −6V (1) |
| | 7 | = | $N_2$ | = supply −6V (2) |
| | 8 | = | | internally connected |
| | 9 | = | P | = supply +6V |
| | 10 | = | E | = common supply 0 V |




Power Supply

| | | | | | | |
|---|---|---|---|---|---|---|
| Terminal | 6 | : | $V_{N1}$ | = −6V ± 2%, | $-I_{N1}$ | = 5.4 mA |
| | 7 | : | $V_{N2}$ | = −6V ± 2%, | $-I_{N2}$ | = 2.2 mA |
| | 9 | : | $V_P$ | = +6V ± 2%, | $I_P$ | = 0.1 – 15 mA |
| | 10 | : | $V_E$ | = 0 V common | | |

MULLARD EQUIPMENT LIMITED

596-1-63

## APPLICATION DATA

The unit is normally used for ferrite-core memory operation in combination with other standard circuit blocks.

### Input (A terminals)

The A terminals are directly connected to the sense output terminals of the core matrix.

### Output (Q terminals)

Output transistor conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = | max. 0.8 V |
| Available current | $-I_Q$ | = | max. 0.5 mA |

Output transistor non-conducting

| | | | |
|---|---|---|---|
| Voltage | $-V_Q$ | = | min. $-0.7\ V_N$ |
| Available current | $I_Q$ | = | max. 1.5 mA |

# SELECTION GATE SG1

**B8 930 05**

**COLOUR CODE: ORANGE**

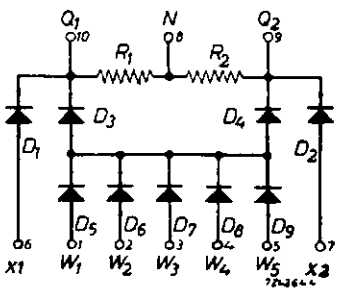
## DATA SHEET

The unit SG1 is designed to perform a two-level AND operation between selection register and selection switches for ferrite-core memory operation.

The first five input AND gates, which decodes the selection register information, is followed by a twin two-input AND gate to perform the Read/Write control function.

The diodes used are germanium types.


| | | | | |
|---|---|---|---|---|
| Terminal | 1 | - $W_1$ - | Selection input 1 |
| | 2 | - $W_2$ - | Selection input 2 |
| | 3 | - $W_3$ - | Selection input 3 |
| | 4 | - $W_4$ - | Selection input 4 |
| | 5 | - $W_5$ - | Selection input 5 |
| | 6 | - $X_1$ - | Read/Write control input 1 |
| | 7 | - $X_2$ - | Read/Write control input 2 |
| | 8 | - N - | Supply -6 V |
| | 9 | - $Q_2$ - | Output 2 |
| | 10 | - $Q_1$ - | Output 1 |




Power supply

Terminal 8 : $V_N$ = -6 V ± 2%, $-I_N$ = 1-2 mA (Nominal value)



MULLARD EQUIPMENT LIMITED

598-1-63

## APPLICATION DATA

The unit is normally used for ferrite-core memory operation, in combination with other standard circuit blocks.

### Selection Input (W terminals)

The W terminals are connected to the flip-flops in the Selection Register. Depending on the size of the memory, this connection may be direct or via adequate amplifier stages.

| | | |
|---|---|---|
| Voltage | $-V_W$ | = max. 0.2 V |
| Required current | $I_W$ | = min. 1 mA at $V_W$ = 0 V |

### Read/Write control input (X terminals)

The $X_1$ and $X_2$ terminals are connected to opposite voltage levels, normally derived from a Read/Write control flip-flop. Depending on the memory capacity, the interconnected $X_1$ resp. $X_2$ terminals are usually driven via a 2.IA1 - 2.1A2 amplifier chain.

| | | |
|---|---|---|
| Voltage | $-V_W$ | = max. 0.2 V |
| Required current | $I_X$ | = min. 1 mA at $V_X$ = 0 V |

### Output (Q terminals)

The Q terminals are directly connected to the W terminals of the driven twin selection switch (2.SS1).

# TWIN SELECTION SWITCH 2.SS1

**B8 960 00**

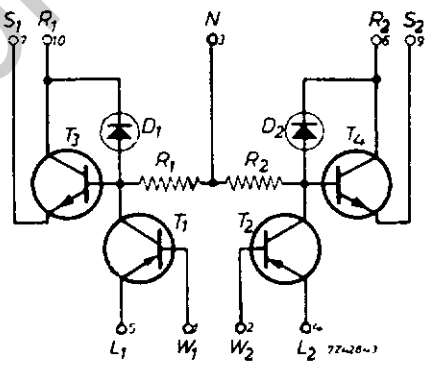
**COLOUR CODE: BLUE**

## DATA SHEET

The unit 2.SS1 contains two identical circuits designed to operate as current switches in series with the drive wires of a ferrite-core memory.

The switching of the n-p-n output transistor is controlled by a d.c. input level applied to the pre-amplifier stage.


| | | | | |
|---|---|---|---|---|
| Terminal | 1 | = $W_1$ | = | control input 1 |
| | 2 | = $W_2$ | = | control input 2 |
| | 3 | = N | = | supply −6 V |
| | 4 | = $L_2$ | = | current input 2 |
| | 5 | = $L_1$ | = | current input 1 |
| | 6 | = $R_2$ | = | switch 2 in |
| | 7 | = $S_1$ | = | switch 1 out |
| | 8 | = | | not connected |
| | 9 | = $S_2$ | = | switch 2 out |
| | 10 | = $R_1$ | = | switch 1 in |




Power Supply

Terminal 3 : $V_N$ = −6 V ± 2%, $-I_N$ = 0–8 mA (Nominal value)



MULLARD EQUIPMENT LIMITED

599–1–63

## APPLICATION DATA

The unit is normally used for ferrite-core memory operation in combination with other standard circuit blocks.

### Control Input (W terminals)

The W terminals are directly connected to the output terminals of the driving SG1.

### Line Input (L terminals)

The L terminals are connected to a current source which can be common to all selection switches operating at the same side of the core matrix.

For the selection switches operating at the negative supply voltage side of the matrix.

Required current $I_L$ = approx. 12 mA

Note: – Usually a 680 Ω± 5% resistor is used between the inter-connected L terminals and the +6 V supply.

For the selection switches operating at the positive supply voltage side of the matrix.

Required current $I_L$ = approx. 18 mA

Limiting value = max. 20 mA

Note: – Usually a grounded base transistor (e.g. type AUY10) with an emitter resistor of approx. 330 Ω is used between the interconnected L terminals and the +6 V supply.

– For memories in which the group selection principle is applied a voltage of max. 1.5V can be tolerated across the drive wire during the switching-on of the drive current.

### Output (R and S terminals)

The output terminals are connected in series with a group of drive wires.

Selection switch conducting

Current $I_{RS}$ = max. 250 mA

Voltage $V_{RS}$ = max. 0.8 V peak value

Selection switch non-conducting

Current $-I_{RS}$ = max. 2.5 mA at $V_{RS}$ = −15V